Hardware Accelerated Collision Detection using Bounded-Error Fixed-Point Arithmetic

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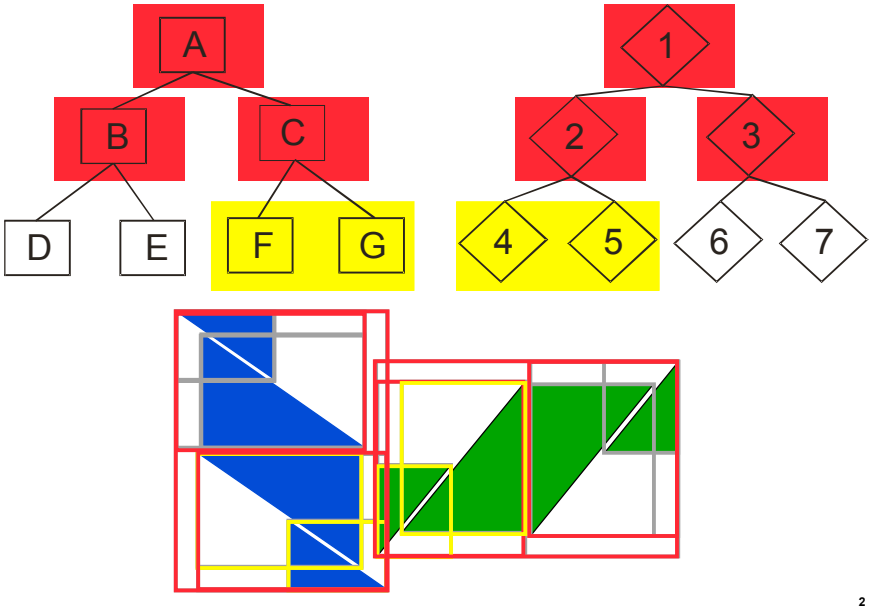
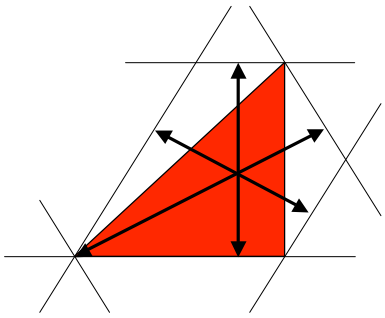
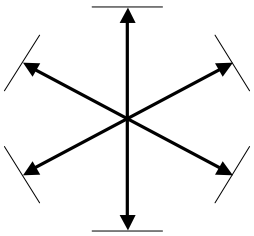
DFG-Project CollisionChip ZA292/2-1
www.collisionchip.de

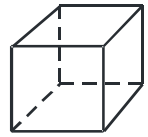
Hierarchical Collision Detection



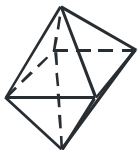
k-DOPs







6-DOP



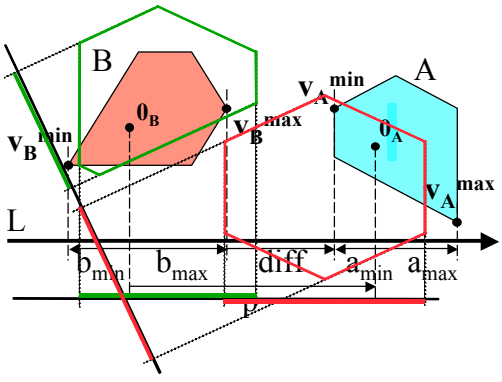
8-DOP

14-DOP

A DOP consists of *k/2* pairs of antiparallel hyperplanes with fixed orientation.

Separating Axis Test (SAT)

- SAT-Algorithm:
  - Choose Testaxis L
  - Project onto L
  - Intervals are separated => BVs are separated



- Mathematics:

$a_{min} = v_A^{min} \cdot L$ $\quad$ $a_{max} = v_A^{max} \cdot L$

$diff_1 = (a_{min} + p) - b_{max}$ $\quad$ $diff_2 = b_{min} - (a_{max} + p)$

Separation on L: $0 < diff = max(diff_1, diff_2)$

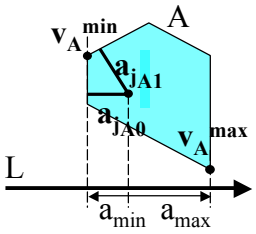
SAT for k-DOPs

- **Individual:**
  - DOP-Coefficients a_i
- **Identical within Hierarchy:**
  - Orientations A_i
  - Correspondencies j_A (A_i of v_A^{min})
- **Mathematics:**

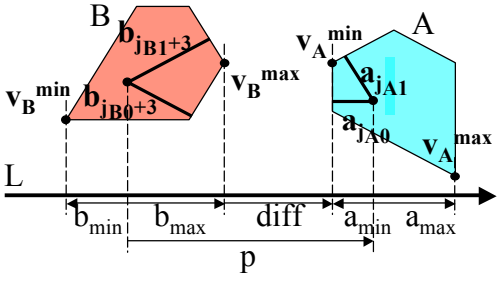
$$v_A^{min} = (a_{jA0}\ a_{jA1}\ a_{jA2}) \cdot (A_{jA0}\ A_{jA1}\ A_{jA2})^{-1}$$

$$a_{min} = v_A^{min} \cdot L = (a_{jA0}\ a_{jA1}\ a_{jA2}) \cdot \underbrace{(A_{jA0}\ A_{jA1}\ A_{jA2})^{-1} \cdot L}_{P_A} = (a_{jA0}\ a_{jA1}\ a_{jA2}) \cdot P_A$$

$$a_{max} = (a_{jA0+k/2}\ a_{jA1+k/2}\ a_{jA2+k/2}) \cdot (-P_A)$$



SAT for k-DOPs (2)



- $diff_1 = (a_{min}+p) - b_{max}$

$$= (a_{jA0}\ a_{jA1}\ a_{jA2}) \cdot P_A + (b_{jB0+k/2}\ b_{jB1+k/2}\ b_{jB2+k/2}) \cdot P_B + p$$

Floating-Point vs. Fixed-Point Arithmetic

Floating-Point			Fixed-Point
–	Large	**Circuit Size**	+ Small
–	Large	**Development overhead**	+ Small
+	High	**Accuracy**	– Low

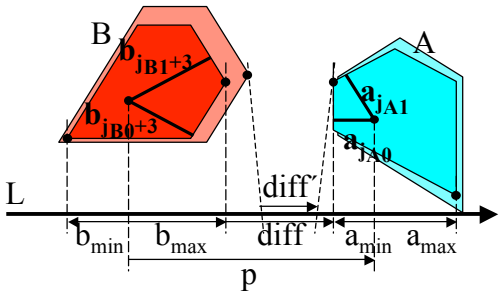
Fixed-Point (Calculation)

- **Rounding of data**

  $p - p' \le 2^{-z}$

  $a_i' - a_i \le 2^{-b}$

  $P_{Ai} - P_{Ai}' \le 2^{-c}$



- **No „false negatives“:**

$diff_1 =$

$(a_{jA0}\ a_{jA1}\ a_{jA2})\cdot P_A + (b_{jB0+k/2}\ b_{jB1+k/2}\ b_{jB2+k/2})\cdot P_B + p$

$diff_1' =$

$(a_{jA0}'\ a_{jA1}'\ a_{jA2}')\cdot P_A' + (b_{jB0+k/2}'\ b_{jB1+k/2}'\ b_{jB2+k/2}')\cdot P_B' + p'$

$+ SN(a_{jA0}'\ a_{jA1}'\ a_{jA2}')\cdot 2^{-c} + SN(b_{jB0+k/2}'\ b_{jB1+k/2}'\ b_{jB2+k/2}')\cdot 2^{-c}$

- **Possible error becomes larger (more „false positives“)**

Fixed-Point (Error-Bound)

- **Rounding**:

$p - p' \le 2^{-z} \qquad a_i' - a_i \le 2^{-b} \qquad P_{Ai} - P_{Ai}' \le 2^{-c}$

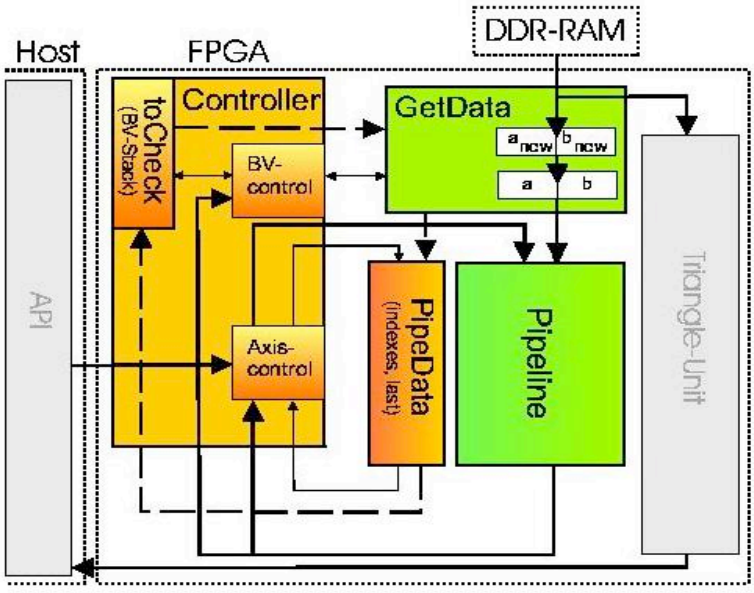
$$diff_1' = (a_{jA0}' \, a_{jA1}' \, a_{jA2}') \cdot P_A' + (b_{jB0+k/2}' \, b_{jB1+k/2}' \, b_{jB2+k/2}') \cdot P_B' + p' + SN(a_{jA0}' \, a_{jA1}' \, a_{jA2}') \cdot 2^{-c} + SN(b_{jB0+k/2}' \, b_{jB1+k/2}' \, b_{jB2+k/2}') \cdot 2^{-c}$$

- **Error-Bound**
  - Assumption: no acute angles between DOP-faces

$$err := diff - diff'$$

$$0 \le err \le \sqrt{3} \cdot 2^{-b+1} + 6 \cdot 2^{-c} + 2^{-z}$$

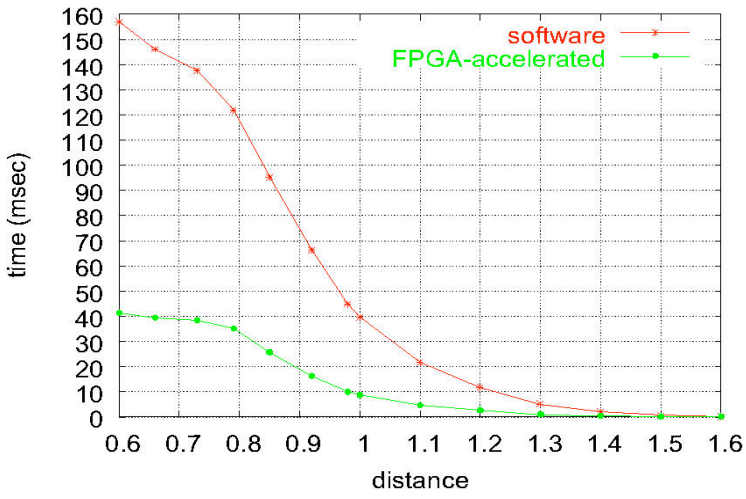
Architecture



Benchmark

- Converge two identical objects
- Rotate one
- Average time to find all intersecting triangles for every distance

Benchmark



- FPGA-Implementation has no cache
- Using FPGA CPU is nearly completely idle

Future Work

- **SAT-Pipeline**
  - Determine optimal choice of parameters
- **Primitives**
  - Triangles
  - Quadrangles
  - NURBS
- **Memory-Interface**
  - Cache
  - Data-Compression
- **Deformable Objects**

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