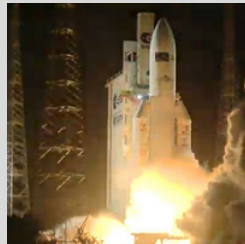


Systems of High Safety and Security

Lecture 1 from 15.10.25: Einführung

Winter term 2025/26



Christoph Lüth

Organisatorisches

Generelles

- ▶ Einführungsvorlesung zum Masterprofil S & Q
- ▶ 6 ETCS-Punkte
- ▶ Vorlesung und Übung:
 - ▶ Mi 10 – 12 Uhr (MZH 1450)
 - ▶ Mi 12 – 14 Uhr (MZH 1450)

- ▶ Material (Folien, Artikel, Übungsblätter) sind auf der Webseite:

`https://user.informatik.uni-bremen.de/~clueth/lehre/ssq.ws25/`

- ▶ Veranstalter:
 - ▶ Christoph Lüth `clueth@uni-bremen.de`
 - ▶ Dieter Hutter (Prüfung) `hutter@uni-bremen.de`

Vorlesung

- ▶ Foliensätze als **Kernmaterial**
 - ▶ Sind auf Englisch (Notationen!)
- ▶ Zusatzmaterial:
 - ▶ Vorlesungsnotizen
 - ▶ Ausgewählte Fachartikel
- ▶ Bücher nur für einzelne Teile der Vorlesung verfügbar:
 - ▶ Nancy Leveson: Engineering a Safer World
 - ▶ Glynn Winskel: The Formal Semantics of Programming Languages
 - ▶ Michael Huth, Mark Ryan: Logic in Computer Science
 - ▶ ... weitere im Laufe der Vorlesung

Übungen

- ▶ Übungsblätter:
 - ▶ “Leichtgewichtige” Übungsblätter, die in der Übung bearbeitet und schnell korrigiert werden können.
 - ▶ Übungsblätter vertiefen Vorlesungsstoff.
 - ▶ Bewertung gibt schnell Feedback.
- ▶ Übungsbetrieb:
 - ▶ Übungsgruppen: bis zu **fünf** (idealerweise drei) Studierende
 - ▶ Bearbeitung: während der Übung
 - ▶ Abgabe: bis zur Vorlesung

Ablauf des Übungsbetriebs

- ▶ Abgabe und Korrektur des Übungsbetriebs erfolgt über **gitlab** .
 - ▶ Dazu legt pro Gruppe ein Repository an.
 - ▶ Ladet mich (clueth) als Developer ein.
- ▶ Für jedes Übungsblatt:
 - ▶ Ihr ladet das Übungsblatt herunter (uebung-XX.md) und bearbeitet es elektronisch.
 - ▶ Die Lösung wird als Markdown in euer Repo abgelegt (dabei Namen uebung-XX.md nicht verändern; Zusatzmaterial als uebung-XX-... wenn nötig), und **vor dem Abgabzeitpunkt** hochgeladen (push).
 - ▶ Nach dem Abgabzeitpunkt laden wir die Abgaben herunter (pull), korrigieren direkt im Markdown, fügen die Bewertung hinzu, und laden die Korrektur wieder hoch (push).
 - ▶ Die Datei 00-BEWERTUNG.md enthält die fortlaufenden Bewertungen für die Gruppe.

Prüfungsleistung

- ▶ Bewertung der Übungen:
 - ▶ A (sehr gut (1.0) – nichts zu meckern, nur wenige Fehler)
 - ▶ B (gut (2.0) – kleine Fehler, im großen und ganzen gut)
 - ▶ C (befriedigend (3.0) – größere Fehler oder Mängel)
 - ▶ Nicht bearbeitet (oder zu viele Fehler)
- ▶ Prüfungsleistung:
 - ▶ Teilnahme am Übungsbetrieb
 - ▶ Eine **Lösung vorstellen** (pro Gruppe)
 - ▶ Mündliche Prüfung am Ende des Semesters
 - ▶ Einzelprüfung, ca. 20- 30 Minuten

Ziel der Vorlesung

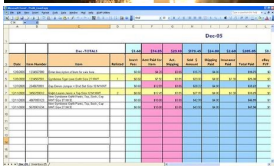
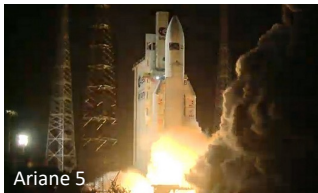
- ▶ Methoden und Techniken zur Entwicklung sicherheitskritischer Systeme
- ▶ Schwerpunkt: formale Methoden
- ▶ Überblick über verschiedene Mechanismen
 - ▶ Vertiefung nach Wahl in verschiedenen Veranstaltungen
- ▶ Verschiedene Dimensionen
 - ▶ Hardware vs. Software
 - ▶ Security vs. Safety

***Formal Methods** refers to mathematically rigorous techniques and tools for the specification, design and verification of software and hardware systems.*

— NASA, <https://shemesh.larc.nasa.gov/fm/fm-what.html>

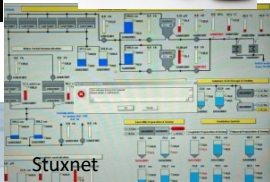
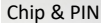
Overview

Why bother with Safety and Security?



Friday October 7, 2011
By Daily Express Reporter

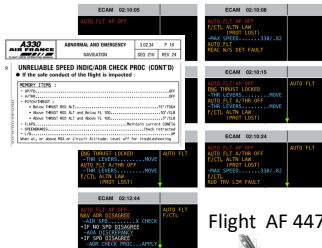
AN accounting error yesterday forced outsourcing specialist Mouchel into a major profits warning and sparked the resignation of its chief executive.



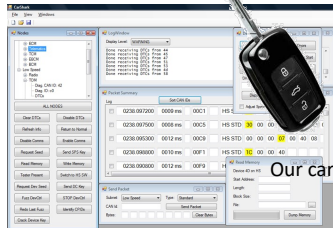
The connection has timed



The server at www.cia.gov is taking too



Flight AF 447



Our car

Cyberattacks on European Airports

- Cause: Ransomware attack on an external service provider.

Technische Probleme

Cyberangriff legt Passagier- und Gepäckabfertigung am Flughafen BER lahm

So 21.09.25 | 17:02 Uhr



Video: rbb24 Abendschau | 20.09.2025 | Charlotte Gehrling | Bild: Picture Alliance/Carsten Koall

Nach einem Cyberangriff führen technische Probleme am BER auch am Sonntag zu längeren Wartezeiten. Passagiere sollen selbst einchecken. Liegendebliebene Gepäckstücke stapeln sich seit Samstag.

The Register



EU's cyber agency blames ransomware as Euro airport check-in chaos continues

Airport staff revert to manual ops as travellers urged to use self-service check-in where possible

Connor Jones

Mon 22 Sep 2025 | 13:11 UTC

The EU's cybersecurity agency today confirmed that ransomware is the cause of continued disruption blighting major airports across Europe.

Aside from the disturbance at various airports including London Heathrow, Berlin Brandenburg, and those in Brussels, Dublin, and Cork, very little is known about the specifics of the attack. No crew has yet claimed responsibility.

The European Union Agency for Cybersecurity (ENISA), sent a statement to *The Register*, saying: "We would like to update you that the cyberattack is confirmed to be a ransomware attack."

The company at the heart of the problems is Collins Aerospace, based in the US, which confirmed cyberattack on Friday evening.

[The Register](#) (above).

[rbb24](#) (left).

Ariane 5

- ▶ Ariane 5 exploded on its virgin flight (Ariane Flight 501) on 4.6.1996.
- ▶ How could that happen?



What Went Wrong With Ariane Flight 501?

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- ⑩ Positioning system was redundant, but both systems failed (systematic error).
- ⑪ Transmission of data to ground control was even unnecessary!

What is Safety and Security?

- ▶ **Safety** is ensured if product achieves acceptable levels of risk or harm to people, business, software, property or the environment in a specified context of use.
- ▶ Threats from “inside”
 - ▶ Avoid malfunction of a system – this concerns both hardware and software
 - ▶ E.g. planes, cars, railways
- ▶ Threats from “outside”
 - ▶ Protect product against force majeure (“acts of god”, “höhere Gewalt”)
 - ▶ E.g. Lightning, storm, floods, earthquake, fatigue of material, loss of power

What is Safety and Security?

- ▶ **Security** is ensured if product is protected against potential attacks from people, environment etc.
- ▶ Protection against threats from “outside”
 - ▶ Analyze and counteract the abilities of an attacker (also called malicious agent).
- ▶ Protection against threats from “inside”
 - ▶ Monitor activities of own personnel, to prevent
 - ▶ selling of sensitive company data
 - ▶ insertion of Trojans during HW/SW design
 - ▶ involuntary misuse
- ▶ In this context: “cybersecurity” (not physical security)

Software Development Models

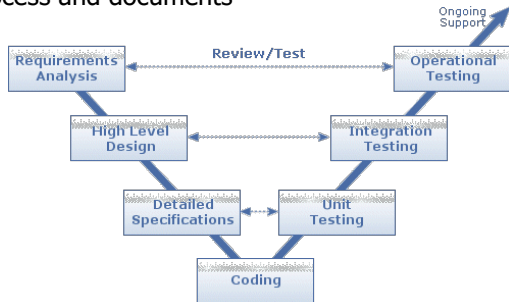
- ▶ Definition of software development process and documents

- ▶ Examples:

- ▶ Waterfall Model
- ▶ **V-Model**
- ▶ Model-Driven Architectures
- ▶ Agile Development

- ▶ Motivation:

- ▶ A well-defined development process is more likely to result in a high-quality product than a chaotic process
- ▶ "Process quality ensures product quality"



Verification and Validation (V&V)

- ▶ **Verification**: have we built the system right?

- ▶ i.e. **correct** with respect to a reference artefact
 - ▶ specification document
 - ▶ reference system
 - ▶ model

*Deutsch:
Korrektheit*

- ▶ **Validation**: have we built the right system?

- ▶ i.e. **effective** (or adequate) for its intended operation?

*Deutsch:
Wirksamkeit*

V&V Methods

▶ **Testing**

- ▶ Test case generation, black- vs. white box
- ▶ Hardware-in-the-loop (HiL) testing: integrated HW/SW system is tested
- ▶ Software-in-the-loop (SiL) testing: only software is tested
- ▶ Program runs using symbolic values (symbolic execution, concolic test)

▶ **Simulation**

- ▶ An executable model is tested with respect to specific properties
- ▶ This is also called Model-in-the-Loop (MiL) testing

▶ Static/dynamic **program analysis**

- ▶ Dependency graphs, flow analysis
- ▶ Symbolic evaluation, abstract interpretation

▶ **Model checking**

- ▶ Automatic proof by reduction to finite state problem

▶ **Formal Verification**

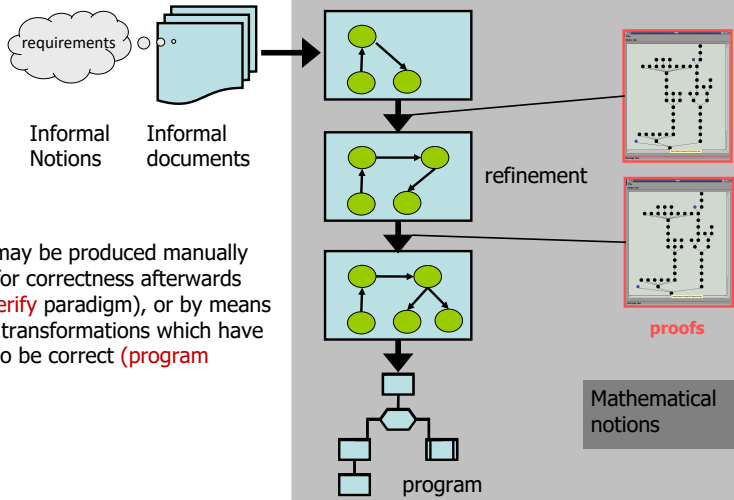
- ▶ Symbolic proof of program properties

Easy to use



Powerful
(Covers all cases)

Formal Software Development



Refinements may be produced manually and checked for correctness afterwards (**invent-and-verify** paradigm), or by means of automated transformations which have been proven to be correct (**program synthesis**)

Concepts of Quality

What is Quality?

- ▶ Quality is the collection of its characteristic properties.
- ▶ Quality model: decomposes the high-level definition by associating attributes (also called characteristics, factors, or **criteria**) to the quality conception.
 - ▶ See Wikipedia for a long list of quality attributes.
- ▶ Quality **indicators** associate **metric values** with **quality criteria** , expressing “how well” the criteria have been fulfilled by the process or product.
 - ▶ The idea is to **measure** quality, with the aim of continuously **improving** it.
 - ▶ Leads to **quality management**
 - ▶ TQM = total quality management
 - ▶ Kaizen = continuous incremental quality improvement
 - ▶ ... but note Goodhart's law:
“When a measure becomes a target, it ceases to be a good measure.”



Quality Criteria: Different Dimensions of Quality

- ▶ For the development of artifacts quality criteria can be measured with respect to the
 - ▶ development process (**process quality**), or
 - ▶ final product (**product quality**).
- ▶ Another dimension for structuring quality conceptions is
 - ▶ **Correctness** (*Korrektheit*): the consistency with the product and its associated requirements specifications, and
 - ▶ **Effectiveness** (*Wirksamkeit*): the suitability of the product for its intended purpose.
- ▶ A third dimension structures quality according to product properties:
 - ▶ **Functional properties** : the specified services to be delivered to the users
 - ▶ **Structural properties** : architecture, interfaces, deployment, control structures
 - ▶ **Non-functional properties** : usability, reliability, availability, security, maintainability, guaranteed worst-case execution time (WCET), costs, absence of run-time errors, ...

Other Norms and Standards

- ▶ ISO 9001 (DIN ISO 9000-4):
 - ▶ Standardizes definition and supporting principles necessary for a quality system to ensure products meet requirements
 - ▶ 'Meta-Standard'
- ▶ CMM (Capability Maturity Model), Spice (ISO 15504)
 - ▶ Standardizes maturity of development process
 - ▶ Level 1 (initial): Ad-hoc
 - ▶ Level 2 (repeatable): process dependent on individuals
 - ▶ Level 3 (defined): process defined & institutionalized
 - ▶ Level 4 (managed): measured process
 - ▶ Level 5 (optimizing): improvement feed back into process

Summary

- ▶ **Safety** vs. **Security**
- ▶ **Quality**
 - ▶ collection of characteristic properties
 - ▶ quality indicators measuring quality criteria
- ▶ Relevant **aspects of quality** here
 - ▶ Functional **suitability** and **safety** (functional correctness)
 - ▶ **Dependability** (availability, reliability, security — non-functional correctness)
- ▶ Next week
 - ▶ Concepts of safety, legal requirements, certification

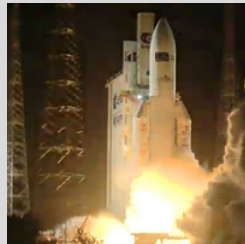
Veranstaltungshinweis

Trustworthy Tuesday (E-Mail follows)

Systems of High Safety and Security

Lecture 2 from 22.10.25: Legal Requirements - Norms and Standards

Winter term 2025/26



Christoph Lüth

Norms and Standards — why bother?

Norms vs. Standards

- ▶ **Norms** are collections of definitions and rules that have been published by one of the standardization bodies, like DIN, ISO, IEC, EN.
- ▶ **Standards** contain the same kinds of information as norms, but have not been published by a standardization body. Examples of standards that are not norms include
 - ▶ HTML (published by ...?)
 - ▶ UML Specifications, published by OMG <https://www.omg.org/spec/UML/2.5.1/About-UML>
 - ▶ C standard (published by ANSI/ISO)
- ▶ In practice both are used interchangeably.

Why bother with norms?

If you want (or need) to write safety-critical software
then you need to adhere to state-of-the-art practice
as specified by the relevant norms and standards.

- ▶ The **bad** news:
 - ▶ As a **qualified professional**, you may become personally liable if you deliberately and intentionally (**grob vorsätzlich**) disregard the state of the art or do not comply to the rules (norms, standards) that were to be applied.
- ▶ The **good** news:
 - ▶ Pay attention here and you will be delivered from these evils.
- ▶ Caution: applies to all kinds of software.

Because in case of failure...

- ▶ Whose fault is it?
- ▶ Who pays for it?
- ▶ Product liability — **Produkthaftung**
 - ▶ European practice: extensive regulation
 - ▶ American practice: litigation (lawsuits)
- ▶ Norms often put a lot of emphasis on process and traceability (auditable evidence): Who decided to do what, why, and how?
- ▶ Which are the relevant norms related to safety and security? → Examples later.

What is Safety?

- ▶ Absolute definition:
 - ▶ “Safety is freedom from accidents or losses.”
 - ▶ Nancy Leveson, “Safeware: System safety and computers”
- ▶ But is there such a thing as absolute safety?
- ▶ Technical definition:
 - ▶ German: “Sicherheit: Freiheit von **unvertretbaren** Risiken”
 - ▶ English: “Safety: Freedom from unjustifiable risks”
 - ▶ IEC 61508-4:2001, §3.1.8

Legal Grounds

- ▶ The **machinery directive** : *The Directive 2006/42/EC of the European Parliament and of the Council of 17 May 2006 on machinery, and amending Directive 95/16/EC (recast)*
- ▶ Scope:
 - ▶ Machineries (with a drive system and movable parts)
- ▶ Objective:
 - ▶ Market harmonization (not safety) – machinery rightfully carrying the CE label is allowed to be sold in all EU countries, regardless of the manufacturer's country
- ▶ Structure:
 - ▶ Sequence of whereas clauses (explanatory)
 - ▶ followed by 29 articles (main body)
 - ▶ and 12 subsequent annexes (detailed information about particular fields, e.g. health & safety)
- ▶ Some application areas have their own regulations:
 - ▶ Cars and motorcycles, railways, planes, nuclear plants ...

The Norms and Standards Landscape

- ▶ First-tier standards (**A-Normen**)
 - ▶ General, widely applicable, no specific area of application
 - ▶ Example: IEC 61508
- ▶ Second-tier standards (**B-Normen**)
 - ▶ Restriction to a particular area of application
 - ▶ Example: ISO 26262 (IEC 61508 for automotive domain)
- ▶ Third-tier standards (**C-Normen**)
 - ▶ Specific pieces of equipment
 - ▶ Example: IEC 61496-3 (“Berührungslos wirkende Schutzeinrichtungen”)
- ▶ Always use most specific norm.

Norms for the Working Programmer

- ▶ **IEC 61508:** *“Functional Safety of Electrical/Electronic/Programmable Electronic Safety-related Systems (E/E/PE, or E/E/PES)”*
 - ▶ Widely applicable, general, considered to be hard to understand
- ▶ **ISO 26262**
 - ▶ Specialisation of 61508 to automotive domain
- ▶ **ISO 21448:** *“Road vehicles – Safety of the intended functionality”*
 - ▶ Complements ISO 26262 for autonomous vehicles using AI algorithms
- ▶ **ANSI/UL 4600:** *“Standard for Safety – Evaluation of Autonomous Products”*
 - ▶ For assuring system-level safety of autonomous systems (cars, railways, aircrafts, robots, . . .)
- ▶ **DIN EN 50128:2012-03**
 - ▶ Specialisation of 61508 to software for railway industry
- ▶ **RTCA DO 178-C:** *“Software Considerations in Airborne Systems and Equipment Certification ”*
 - ▶ Airplanes, NASA/ESA

- ▶ **ISO 15408:** *“Common Criteria for Information Technology Security Evaluation”*
 - ▶ Security, evolved from TCSEC (“Orange Book”, US), ITSEC (EU), CTCPEC (Canada)
 - ▶ Must be applied for security-relevant systems or products used in military or public administration.
- ▶ **IEC 62443:** *“Industrial communication networks – IT security for networks and systems”*
 - ▶ Practical alternative to ISO 15408 for industrial applications

Functional Safety: IEC 61508 and friends

What is regulated by IEC 61508?

- ▶ Analyse the operation of the **unprotected system**.
- ▶ What is the risk that could occur if the system is operated **without protection**?
- ▶ If this risk is too high, introduce a **safety controller** (also called **safety supervisor**) which may be realised as an electric, electronic or programmable electronic system (E/E/PES) and performs a safety function.
 - ▶ The system to be operated with the safety controller becomes the Equipment Under Control (EUC).
- ▶ Now the safety controller **could fail** when needed.
 - ▶ Therefore, the safety controller must be developed with **greater care** if its **failure** may result in **higher risks**.
 - ▶ Therefore, the safety controller needs to be developed according to a certain **safety integrity level** (SIL).

The Standard Approach to Safety of IEC 61508

- ▶ **Risk analysis** determines the safety integrity level (SIL).
- ▶ **Hazard analysis** leads to **safety requirement** specification.
- ▶ **Safety requirements** must be satisfied by product:
 - ▶ Need to **verify** that this is achieved.
 - ▶ SIL determines amount of development documentation and V&V effort
- ▶ **Life-cycle** needs to be managed and organised:
 - ▶ Planning: development plan, verification & validation plan ...
 - ▶ Note: personnel needs to be qualified.
- ▶ All of this needs to be **independently assessed** by verification and validation (V&V) teams, certification authorities whose personnel are called safety assessors.
 - ▶ SIL determines the required independence of assessment body.

Definition: Safety Integrity

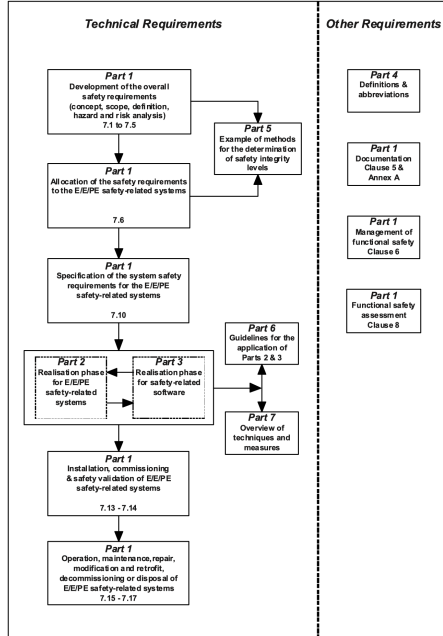
- ▶ Safety integrity is defined as the probability of a safety-related system to satisfactorily perform the required safety functions under all the stated conditions within a stated period of time.
- ▶ Safety integrity does not say anything about the availability or reliability of end-user functionality, if the latter is not safety-related.
- ▶ Definitions of reliability and availability:
 - ▶ Availability = probability of the system to be usable with its specified services when it is needed;
 - ▶ Reliability = probability of the system to perform its specified services while it is used.

The Seven Parts of IEC 61508

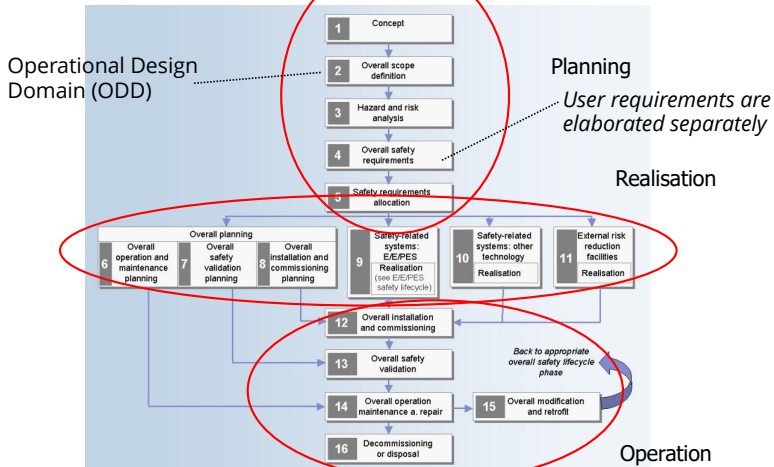
Electric / Electronic / Programmable Electronic Software

- ▶ General requirements
- ▶ Requirements for E/E/PES safety-related systems
 - ▶ Hardware rather than software
- ▶ **Software requirements**
- ▶ Definitions and abbreviations
- ▶ Examples of methods for the determination of safety-integrity levels
 - ▶ **Mostly informative**
- ▶ Guidelines on the application of Part 2 and 3
 - ▶ **Mostly informative**
- ▶ Overview of techniques and measures

The Seven Parts of IEC 61508



The Safety Life Cycle (IEC 61508)



E/E/PES: Electrical/Electronic/Programmable Electronic Safety-related Systems

Risk Definitions

- ▶ The most general definition of risk – also given in IEC 61508 – is as follows.
 - ▶ Risk is the combination of the probability of occurrence of harm and the severity of harm
- ▶ Two frequently applied formulas are
 - ▶ Risk = probability-of-occurrence-of-harm * cost-of-resulting-harm
 - ▶ Risk = frequency-of-occurrence-of-harm * cost-of-resulting-harm
- ▶ Probability and frequency are always expressed as **scalar value per time unit** , typically **value/hour** or **value/year**

The Safety Integrity Level

Safety Integrity Levels

Maximum tolerable risk exposure

- ▶ What is the risk of operating a system?
- ▶ Two factors:
 - ▶ How likely is a failure ?
 - ▶ What is the damage caused by a failure?



Numerical Characteristics of Safety Integrity Level

- ▶ The standard IEC 61508 defines the following numerical characteristics per safety integrity level:
 - ▶ **PFD**, average Probability of Failure to perform its designed function on Demand (average probability of dangerous failure on demand of the safety function), i.e. the probability of unavailability of the safety function leading to dangerous consequences.
 - ▶ **PFH**, the Probability of a dangerous Failure per Hour (average frequency of dangerous failure of the safety function).
- ▶ Failure on demand = “function fails when it is needed”

Safety Integrity Level (SIL)

- ▶ The SIL defines the **probability** that the safety control function **fails** to perform its function (on demand).
- ▶ The higher the SIL, the more strictly development, verification, and validation methods must be regulated and documented; and development personnel must be higher qualified.
- ▶ Maximum average probability of a **dangerous failure** (per hour/per demand) is determined depending on how often it is used:
 - ▶ **Low demand** of the safety function: at most once per year \rightarrow max. PFD
 - ▶ Example: Airbag and its controller
 - ▶ **High demand**: more than once per year \rightarrow max. PFH
 - ▶ Example 1: Car brakes (demand still occurs at discrete points in time)
 - ▶ Example 2: Safety function of autonomous vehicle (continuous demand)

Safety Integrity Level and PFD/PFH

- ▶ The following table correlates the SIL to the max. PFD/PFH:

SIL	High Demand (more than once a year)	Low Demand (once a year or less)
4	$10^{-9} < \text{PFH}/\text{h} < 10^{-8}$	$10^{-5} < \text{PFD}_{\text{avg}} < 10^{-4}$
3	$10^{-8} < \text{PFH}/\text{h} < 10^{-7}$	$10^{-4} < \text{PFD}_{\text{avg}} < 10^{-3}$
2	$10^{-7} < \text{PFH}/\text{h} < 10^{-6}$	$10^{-3} < \text{PFD}_{\text{avg}} < 10^{-2}$
1	$10^{-6} < \text{PFH}/\text{h} < 10^{-5}$	$10^{-2} < \text{PFD}_{\text{avg}} < 10^{-1}$

- ▶ How to read this table: e.g. if we develop a safety function with SIL 3, we can (reasonably) assume it fails once between 10000 and 1000 years.

Establishing target SIL (Quantitative)

- ▶ IEC 61508 does not describe a standard procedure to establish a SIL target, it allows for alternatives.
- ▶ Quantitative approach:
 - ▶ Start with target risk level (maximal tolerable risk)
 - ▶ Factor in fatality and frequency
 - ▶ Develop system with such a SIL that target risk level is not superceded.

Maximum tolerable risk of fatality	Individual risk (per annum)
Employee	10^{-4}
Public	10^{-5}
Broadly acceptable ("Negligible")	10^{-6}

Establishing target SIL (Quantitative)

- ▶ Establish maximal tolerable risk of fatality A
- ▶ Establish probability of hazardous events leading to fatality B
- ▶ Determine low or high demand, and establish risk of failure (i.e. a hazardous state is entered) of **unprotected** process C ; determine
- ▶ Risk of fatality, unprotected is $B \cdot C$.
- ▶ If $B \cdot C > A$, then we need a **safety function**. This will have a probability of failure of E .
- ▶ The risk of fatality, protected, is $E \cdot B \cdot C$. E must be so low that $E \cdot B \cdot C \leq A$, so E can be computed as

$$E \leq \frac{A}{B \cdot C}$$

- ▶ Now lookup E in table on previous slide to determine SIL. E is PFH/h with high demand, or PFD_{avg} with low demand.

Example: Safety system for a chemical plant

- ▶ Max. tolerable risk exposure: $A = 10^{-6}$ (per annum)
- ▶ Probability of hazardous events leading to fatality: $B = 10^{-2}$
- ▶ Risk of failure of unprotected process: $C = \frac{1}{5}$ per annum (once in 5 years),
 - ▶ The probability that the safety-function needs to kick in is less than once per year: we can determine the SIL-level according to the low demand column.
- ▶ Risk of fatality, unprotected: $B \cdot C = 2 \cdot 10^{-3}$ (once in 500 years)
- ▶ Since $B \cdot C > A$, we need safety function with $E \leq \frac{A}{B \cdot C} = 5 \cdot 10^{-4}$
- ▶ Lookup E in table in low demand colum: **SIL 3.**

Example: Safety system for a hydraulic press

- ▶ Max. tolerable risk exposure: $A=10^{-4}$ per annum, i.e. $A' = 10^{-8}$ per hour
- ▶ Ratio of hazardous events leading to serious injury: $B = \frac{1}{100}$.
 - ▶ Worker will not wilfully put his hands into the press.
- ▶ Risk of failure of unprotected process: $C = 50$ per hour.
 - ▶ Press operates and pushes down on work item 50 times/hour.
 - ▶ This means that protection mechanism is needed more often than once per year: high demand of safety function.
- ▶ Risk of fatality, unprotected: $B \cdot C = \frac{50}{100} = \frac{1}{2}$ per hour
- ▶ Clearly $B \cdot C > A'$, so we need safety function with $E \leq \frac{A'}{B \cdot C} = 2 \cdot 10^{-8}$.
- ▶ Lookup E in high demand column: **SIL 3**.

Example: Heating iron (or similar domestic appliance)

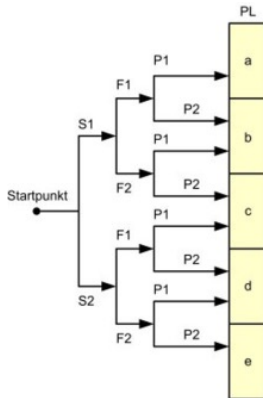
- ▶ Overheating may cause fire.
- ▶ Max. tolerable risk exposure: $A = 10^{-5}$ per annum, i.e. $A' = 10^{-9}$ per hour.
- ▶ Study suggests 1 in 400 incidents leads to fatality, i.e. $B \cdot C = \frac{1}{400}$.
- ▶ High demand for safety controller, because heating iron is used very often.
- ▶ Since $B \cdot C > A'$, we need safety function with $E \leq \frac{A'}{B \cdot C} = 10^{-9} \cdot 400 = 4 \cdot 10^{-7}$.
- ▶ Lookup E in table high demand column: **SIL 2**.

Establishing Target SIL (Qualitative)

- Qualitative method: **risk graph analysis** (e.g. DIN 13849).
- DIN EN ISO 13849:1 determines the **performance level (PL)**.

PL	SIL
a	-
b	1
c	2
d	3
e	4

Relation PL to SIL



Source: Peter Wratil (Wikipedia)

Severity of injury:

S1 - slight (reversible) injury

S2 - severe (irreversible) injury

Occurrence:

F1 - rare occurrence

F2 - frequent occurrence

Possible avoidance:

P1 - possible

P2 - impossible

What are the implications of SIL for the development process?

▶ In general:

- ▶ “Competent” personnel
- ▶ Independent assessment (“four eyes”)

▶ SIL 1:

- ▶ Basic quality assurance (e.g. ISO 9001).

▶ SIL 2:

- ▶ Safety-directed quality assurance, more tests.

▶ SIL 3:

- ▶ Exhaustive testing, possibly formal methods.
- ▶ Assessment by separate department.

▶ SIL 4:

- ▶ State-of-the-art practices, formal methods.
- ▶ Assessment by separate organization

Different Norms have differing notions of safety integrity

Approximate cross-domain mapping of ASIL

Domain	Domain-Specific Safety Levels					
Automotive (ISO 26262)	QM	ASIL A	ASIL B	ASIL C	ASIL D	-
General (IEC 61508)	-	SIL-1	SIL-2		SIL-3	SIL-4
Railway (CENELEC 50126/128/129)	-	SIL-1	SIL-2		SIL-3	SIL-4
Space (ECSS-Q-ST-80)	Category E	Category D	Category C		Category B	Category A
Aviation: airborne (ED-12/DO-178/DO-254)	DAL-E	DAL-D	DAL-C		DAL-B	DAL-A
Aviation: ground (ED-109/DO-278)	AL6	AL5	AL4	AL3	AL2	AL1
Medical (IEC 62304)	Class A	Class B			Class C	-
Household (IEC 60730)	Class A	Class B			Class C	-
Machinery (ISO 13849)	PL a	PL b	PL c	PL d		PL e
						-

Source: https://en.wikipedia.org/wiki/Automotive_Safety_Integrity_Level

Some Terminology

- ▶ Error handling:
 - ▶ Fail-safe (or fail-stop): terminate in a safe state.
 - ▶ Fail-operational systems: continue operation, even if (some) controllers fail.
 - ▶ Fault-tolerant systems: continue with a potentially degraded service (more general than fail operational systems)
- ▶ Safety-critical, safety-relevant (German: *sicherheitskritisch*)
 - ▶ General term – failure may lead to risk
- ▶ Safety function (German: *Sicherheitsfunktion*)
 - ▶ Technical term, the part of the functionality that ensures safety
- ▶ Safety-related (German: *sicherheitsgerichtet, sicherheitsbezogen*)
 - ▶ Technical term, directly related to the safety function

Increasing SIL by redundancy

- ▶ One can achieve a higher SIL by combining **independent** systems with lower SIL (*Mehrkanalsysteme*).
- ▶ Given two systems A , B with failure probabilities P_A , P_B the chance for failure of both is (with P_{CC} probability of common-cause failures): $P_{AB} = P_{CC} + P_AP_B$
- ▶ Hence, combining two SIL 3 systems **may** give you a SIL 4 system.
- ▶ However, be aware of **systematic** errors (and note that IEC 61508 considers all software errors to be systematic) — these result in common-cause failures.
- ▶ Note also that for fail-operational systems you need three (not two) systems.
- ▶ The degree of independence can be increased by **software diversity**: channels are equipped with software following the same specification but developed by independent teams

The Software Development Process

- ▶ 61508 in principle allows any software lifecycle model, but:
 - ▶ No specific process model is given, illustrations use a V-model, and no other process model is mentioned.
- ▶ Appx A, B give normative guidance on measures to apply:
 - ▶ Error detection needs to be taken into account (e.g. runtime assertions, error detection codes, dynamic supervision of data/control flow)
 - ▶ Use of strongly typed programming languages (see table)
 - ▶ Discouraged use of certain features:
 - ▶ recursion(!), dynamic memory, unrestricted pointers, unconditional jumps
 - ▶ **Certified** (also called **qualified** or **validated**) tools and compilers must be used or tools “proven in use”.

Proven in Use: Statistical Evaluation

- ▶ As an alternative to systematic development, statistics about usage may be employed. This is particularly relevant:
 - ▶ for development tools (compilers, verification tools etc),
 - ▶ and for re-used software (modules, libraries).
- ▶ The norm (61508-7 Appx. D) is quite brief about this subject. It states these methods should only be applied by those “competent in statistical analysis”.
- ▶ The problem: proper statistical analysis is more than just “plugging in numbers”.
 - ▶ Previous use needs to be to the same specification as intended use (e.g. compiler: same target platform).
 - ▶ Uniform distribution of test data, independent tests.
 - ▶ Perfect detection of failure.
- ▶ The rapid change of technology makes it frequently impossible to gather reliable statistic data about tools or HW components.
 - ▶ Therefore, “proven in use approach” is not often possible to be applied.

Table A.2 - Software Architecture

**Table A.2 – Software design and development –
software architecture design**

(see 7.4.3)

	Technique/Measure *	Ref.	SIL 1	SIL 2	SIL 3	SIL 4
	Architecture and design feature					
1	Fault detection	C.3.1	---	R	HR	HR
2	Error detecting codes	C.3.2	R	R	R	HR
3a	Failure assertion programming	C.3.3	R	R	R	HR
3b	Diverse monitor techniques (with independence between the monitor and the monitored function in the same computer)	C.3.4	---	R	R	----
3c	Diverse monitor techniques (with separation between the monitor computer and the monitored computer)	C.3.4	---	R	R	HR
3d	Diverse redundancy, implementing the same software safety requirements specification	C.3.5	---	---	---	R
3e	Functionally diverse redundancy, implementing different software safety requirements specification	C.3.5	---	---	R	HR
3f	Backward recovery	C.3.6	R	R	---	NR
3g	Stateless software design (or limited state design)	C.2.12	---	---	R	HR
4a	Re-try fault recovery mechanisms	C.3.7	R	R	---	---
4b	Graceful degradation	C.3.8	R	R	HR	HR
5	Artificial intelligence - fault correction	C.3.9	---	NR	NR	NR
6	Dynamic reconfiguration	C.3.10	---	NR	NR	NR

Table A.2 - Software Architecture

7	Modular approach	Table B.9	HR	HR	HR	HR
8	Use of trusted/verified software elements (if available)	C.2.10	R	HR	HR	HR
9	Forward traceability between the software safety requirements specification and software architecture	C.2.11	R	R	HR	HR
10	Backward traceability between the software safety requirements specification and software architecture	C.2.11	R	R	HR	HR
11a	Structured diagrammatic methods **	C.2.1	HR	HR	HR	HR
11b	Semi-formal methods **	Table B.7	R	R	HR	HR
11c	Formal design and refinement methods **	B.2.2, C.2.4	---	R	R	HR
11d	Automatic software generation	C.4.6	R	R	R	R
12	Computer-aided specification and design tools	B.2.4	R	R	HR	HR
13a	Cyclic behaviour, with guaranteed maximum cycle time	C.3.11	R	HR	HR	HR
13b	Time-triggered architecture	C.3.11	R	HR	HR	HR
13c	Event-driven, with guaranteed maximum response time	C.3.11	R	HR	HR	-
14	Static resource allocation	C.2.6.3	-	R	HR	HR
15	Static synchronisation of access to shared resources	C.2.6.3	-	-	R	HR

Table A.4 - Software Design & Development

**Table A.4 – Software design and development –
detailed design**

(See 7.4.5 and 7.4.6)

(Includes software system design, software module design and coding)

Technique/Measure *		Ref.	SIL 1	SIL 2	SIL 3	SIL 4
1a	Structured methods **	C.2.1	HR	HR	HR	HR
1b	Semi-formal methods **	Table B.7	R	HR	HR	HR
1c	Formal design and refinement methods **	B.2.2, C.2.4	---	R	R	HR
2	Computer-aided design tools	B.3.5	R	R	HR	HR
3	Defensive programming	C.2.5	---	R	HR	HR
4	Modular approach	Table B.9	HR	HR	HR	HR
5	Design and coding standards	C.2.6 Table B.1	R	HR	HR	HR
6	Structured programming	C.2.7	HR	HR	HR	HR
7	Use of trusted/verified software elements (if available)	C.2.10	R	HR	HR	HR
8	Forward traceability between the software safety requirements specification and software design	C.2.11	R	R	HR	HR

Table A.5 – SW Design and Development

Table A.5 – Software design and development – software module testing and integration

(See 7.4.7 and 7.4.8)

Technique/Measure *		Ref.	SIL 1	SIL 2	SIL 3	SIL 4
1	Probabilistic testing	C.5.1	---	R	R	R
2	Dynamic analysis and testing	B.6.5 Table B.2	R	HR	HR	HR
3	Data recording and analysis	C.5.2	HR	HR	HR	HR
4	Functional and black box testing	B.5.1 B.5.2 Table B.3	HR	HR	HR	HR
5	Performance testing	Table B.6	R	R	HR	HR
6	Model based testing	C.5.27	R	R	HR	HR
7	Interface testing	C.5.3	R	R	HR	HR
8	Test management and automation tools	C.4.7	R	HR	HR	HR
9	Forward traceability between the software design specification and the module and integration test specifications	C.2.11	R	R	HR	HR
10	Formal verification	C.5.12	---	---	R	R

[illegible]

Table A.6 – Programmable Electronics Integration (HW/SW)

Table A.6 – Programmable electronics integration (hardware and software)

(See 7.5)

Technique/Measure *		Ref.	SIL 1	SIL 2	SIL 3	SIL 4
1	Functional and black box testing	B.5.1 B.5.2 Table B.3	HR	HR	HR	HR
2	Performance testing	Table B.6	R	R	HR	HR
3	Forward traceability between the system and software design requirements for hardware/software integration and the hardware/software integration test specifications	C.2.11	R	R	HR	HR

Table A.7 - Software Aspects of System Safety Validation

Table A.7 – Software aspects of system safety validation

(See 7.7)

Technique/Measure *		Ref.	SIL 1	SIL 2	SIL 3	SIL 4
1	Probabilistic testing	C.5.1	---	R	R	HR
2	Process simulation	C.5.18	R	R	HR	HR
3	Modelling	Table B.5	R	R	HR	HR
4	Functional and black-box testing	B.5.1 B.5.2 Table B.3	HR	HR	HR	HR
5	Forward traceability between the software safety requirements specification and the software safety validation plan	C.2.11	R	R	HR	HR
6	Backward traceability between the software safety validation plan and the software safety requirements specification	C.2.11	R	R	HR	HR

NOTE 1: See Table C.7

Table A.9 – Software Verification

Table A.9 – Software verification

(See 7.9)

Technique/Measure *		Ref.	SIL 1	SIL 2	SIL 3	SIL 4
1	Formal proof	C.5.12	---	R	R	HR
2	Animation of specification and design	C.5.26	R	R	R	R
3	Static analysis	B.6.4 Table B.8	R	HR	HR	HR
4	Dynamic analysis and testing	B.6.5 Table B.2	R	HR	HR	HR
5	Forward traceability between the software design specification and the software verification (including data verification) plan	C.2.11	R	R	HR	HR
6	Backward traceability between the software verification (including data verification) plan and the software design specification	C.2.11	R	R	HR	HR
7	Offline numerical analysis	C.2.13	R	R	HR	HR
Software module testing and integration		See Table A.5				
Programmable electronics integration testing		See Table A.6				
Software system testing (validation)		See Table A.7				

Table B.1 – Coding Guidelines

**Tabelle B.1 – Entwurfs- und Codierungs-Richtlinien
(Verweisungen aus Tabelle A.4)**

	Verfahren/Maßnahme *	siehe	SIL1	SIL2	SIL3	SIL4
1	Verwendung von Codierungs-Richtlinien	C.2.6.2	++	++	++	++
2	Keine dynamischen Objekte	C.2.6.3	+	++	++	++
3a	Keine dynamischen Variablen	C.2.6.3	o	+	++	++
3b	Online-Test der Erzeugung von dynamischen Variablen	C.2.6.4	o	+	++	++
4	Eingeschränkte Verwendung von Interrupts	C.2.6.5	+	+	++	++
5	Eingeschränkte Verwendung von Pointern	C.2.6.6	o	+	++	++
6	Eingeschränkte Verwendung von Rekursionen	C.2.6.7	o	+	++	++
7	Keine unbedingten Sprünge in Programmen in höherer Programmiersprache	C.2.6.2	+	++	++	++
ANMERKUNG 1 Die Maßnahmen 2 und 3a brauchen nicht angewendet zu werden, wenn ein Compiler verwendet wird, der sicherstellt, dass genügend Speicherplatz für alle dynamischen Variablen und Objekte vor der Laufzeit zugeteilt wird, oder der Laufzeittests zur korrekten Online-Zuweisung von Speicherplatz einfügt.						
* Es müssen dem Sicherheits-Integritätslevel angemessene Verfahren/Maßnahmen ausgewählt werden. Alternative oder gleichwertige Verfahren/Maßnahmen sind durch einen Buchstaben hinter der Nummer gekennzeichnet. Es muss nur eine(s) der alternativen oder gleichwertigen Verfahren/Maßnahmen erfüllt werden.						

- ▶ Table C.1, programming languages, mentions:
 - ▶ ADA, Modula-2, Pascal, FORTRAN 77, C, PL/M, Assembler, ...
- ▶ Example for a guideline:
 - ▶ MISRA-C: 2023, Guidelines for the use of the C language in critical systems.

Table B.5 - Modelling

**Tabelle B.5 – Modellierung
(Verweisung aus der Tabelle A.7)**

Verfahren/Maßnahme *	siehe	SIL1	SIL2	SIL3	SIL4
1 Datenflussdiagramme	C.2.2	+	+	+	+
2 Zustandsübergangsdiagramme	B.2.3.2	o	+	++	++
3 Formale Methoden	C.2.4	o	+	+	++
4 Modellierung der Leistungsfähigkeit	C.5.20	+	++	++	++
5 Petri-Netze	B.2.3.3	o	+	++	++
6 Prototypenerstellung/Animation	C.5.17	+	+	+	+
7 Strukturdiagramme	C.2.3	+	+	+	++
ANMERKUNG Sollte eine spezielles Verfahren in dieser Tabelle nicht vorkommen, darf nicht angenommen werden, dass dieses nicht in Betracht gezogen werden darf. Es sollte zu dieser Norm in Einklang stehen.					
* Es müssen dem Sicherheits-Integritätslevel angemessene Verfahren/Maßnahmen ausgewählt werden.					

Certification

- ▶ **Certification** is the process of showing **conformance** to a **standard**.
- ▶ Conformance to IEC 61508 can be shown in two ways:
 - ▶ either that an organization (company) has in principle the ability to produce a product conforming to the standard,
 - ▶ or that a specific product (or system design) conforms to the standard.
- ▶ Certification can be done by the developing company (self-certification) but is typically done by a **notified body** (“benannte Stellen”).
 - ▶ In Germany, e.g. the TÜVs or **Berufsgenossenschaften** ;
 - ▶ In Britain, professional role (ISA) supported by IET/BCS;
 - ▶ Aircraft certification in Europe: EASA (European Aviation Safety Agency)
 - ▶ Aircraft certification in US: FAA (Federal Aviation Administration)

An Important New Trend

- ▶ Until recently, software components contributing to a safety function had to be developed in a way ensuring that the probability of remaining software bugs could be neglected (formal verification, exhaustive testing). It was not allowed to leave a known bug inside the SW and argue that the risk induced by this bug is small enough to be neglected.
- ▶ With the advent of autonomous systems (in particular, road vehicles and robots), AI-related methods were implemented in software, such as neural networks for traffic sign recognition. This type of software components has two new characteristics:
 - ① It performs correctly only with a certain probability.
 - ② It may change its behaviour over time, due to effects of runtime machine learning.
- ▶ The standards in the automotive domain are already being adapted: ISO 21448; other standards will follow. This trend comes with a considerable risk: In the future, the probabilistic argument might also be applied to buggy software which should better be corrected.

Conclusion

Summary

- ▶ Norms and standards enforce the application of the state-of-the-art when developing software which is **safety-critical** or **security-critical**.
- ▶ Wanton disregard of these norms may lead to **personal liability**.
- ▶ Norms typically place a lot of emphasis on **process**.
- ▶ Key question are **traceability** of decisions and design, and **verification** and **validation**.
- ▶ Different application fields have different norms:
 - ▶ **Safety**: IEC 61508 and its specializations, e.g. ISO 26262, DO-178 B/C.
 - ▶ **Security**: IEC 15408 (“Common Criteria”)

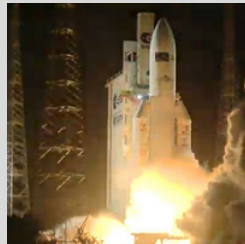
Further Reading

- ▶ Terminology for dependable systems:
 - ▶ J. C. Laprie *et al.*: Dependability: Basic Concepts and Terminology. Springer-Verlag, Berlin Heidelberg New York (1992).
- ▶ Literature on safety-critical systems:
 - ▶ Storey, Neil: Safety-Critical Computer Systems. Addison Wesley Longman (1996).
 - ▶ Nancy Levenson: Safeware – System Safety and Computers. Addison-Wesley (1995).
- ▶ A readable introduction to IEC 61508:
 - ▶ David Smith and Kenneth Simpson: Functional Safety. 2nd Edition, Elsevier (2004).

Systems of High Safety and Security

Lecture 3 from 29.10.2025: The Development Process

Winter term 2025/26



Christoph Lüth

Organisatorisches

- ▶ Die Vorlesung und Übung am 05.11.2025 **fällt aus.**

Software Development Models

Software Development Process

- ▶ A software development process is the **structure** imposed on the development of a software product.
- ▶ We classify processes according to **models** which specify
 - ▶ the artefacts of the development: the software product itself, specifications, test documents, reports, reviews, proofs, plans etc;
 - ▶ the different stages of the development;
 - ▶ and the artefacts associated to each stage.
- ▶ Different models have a different focus: correctness, development time, flexibility.
 - ▶ Note you cannot have all three
- ▶ What does **quality** mean in this context?
 - ▶ What is the **output** — just the software product, or more? (specifications, test runs, documents, proofs. . .)

Artefacts in the Development Process

Planning:

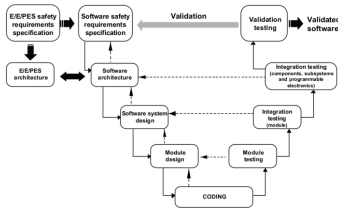
- ▶ Document plan
- ▶ V&V plan
- ▶ QM plan
- ▶ Test plan
- ▶ Project manual

Specifications:

- ▶ Requirements
- ▶ System specification
- ▶ Module specification
- ▶ User documents

Implementation:

- ▶ Source code
- ▶ Models
- ▶ Documentation



Verification & validation:

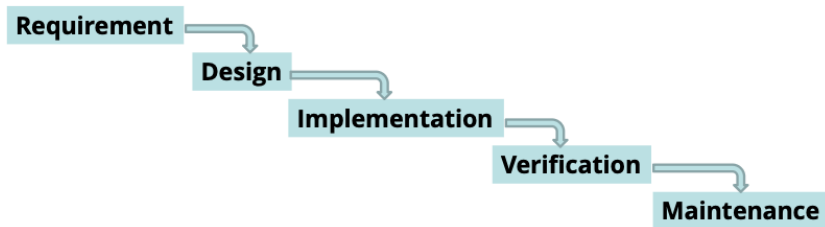
- ▶ Code review protocols
- ▶ Test cases, test results
- ▶ Proofs

Possible formats:

- ▶ Documents:
 - ▶ Word/LaTeX documents
 - ▶ Excel sheets
 - ▶ Wiki text
 - ▶ Database (Doors)
- ▶ Models:
 - ▶ UML/SysML diagrams
 - ▶ Formal languages: Z, HOL, B, etc.
 - ▶ Matlab/Simulink or similar diagrams
- ▶ Source code

Waterfall Model (Royce 1970)

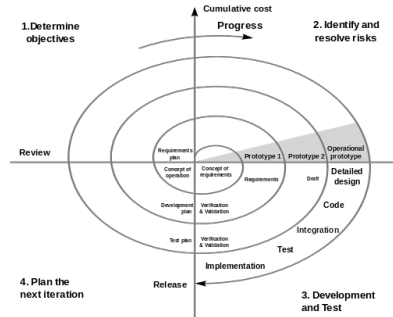
- ▶ Classical top-down sequential workflow with strictly separated phases.



- ▶ Unpractical as an actual workflow (no feedback between phases), but even the original paper did **not** really suggest this.

Spiral Model (Böhm 1986)

- ▶ Incremental development guided by **risk factors**
- ▶ Four phases:
 - ▶ Determine objectives
 - ▶ Analyse risks
 - ▶ Development and test
 - ▶ Review, plan next iteration
- ▶ See e.g.
 - ▶ Rational Unified Process (RUP)
- ▶ Drawbacks:
 - ▶ Risk identification is the key, and can be quite difficult



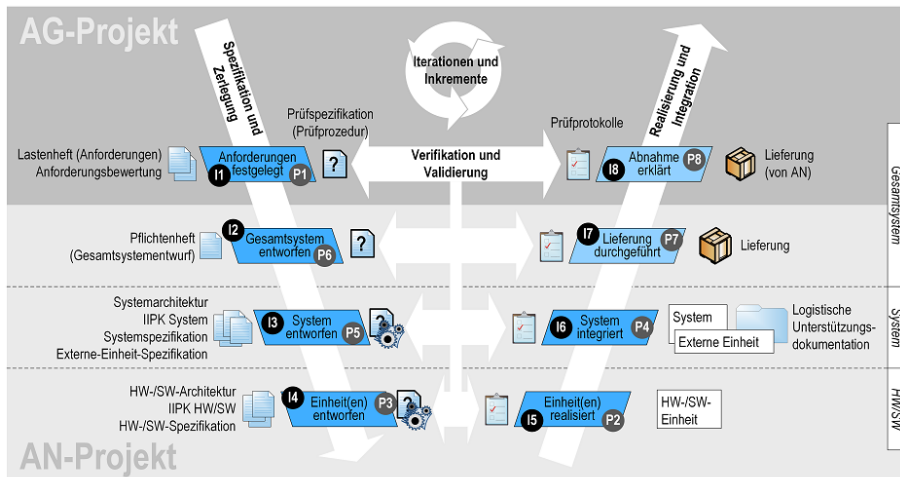
Agile Methods

- ▶ **Prototype-driven** development
 - ▶ e.g. Rapid Application Development
 - ▶ Development as a sequence of prototypes
 - ▶ Ever-changing safety and security requirements
- ▶ **Agile programming**
 - ▶ e.g. extreme Programming (XP), Scrum
 - ▶ Development guided by functional requirements
 - ▶ Process structured by rules of conduct for developers
 - ▶ Rules capture best practice
 - ▶ Less support for non-functional requirements
- ▶ **Test-driven development (TDD)**
 - ▶ Tests as **executable specifications**: write tests first
 - ▶ Often used together with the other two

V-Model

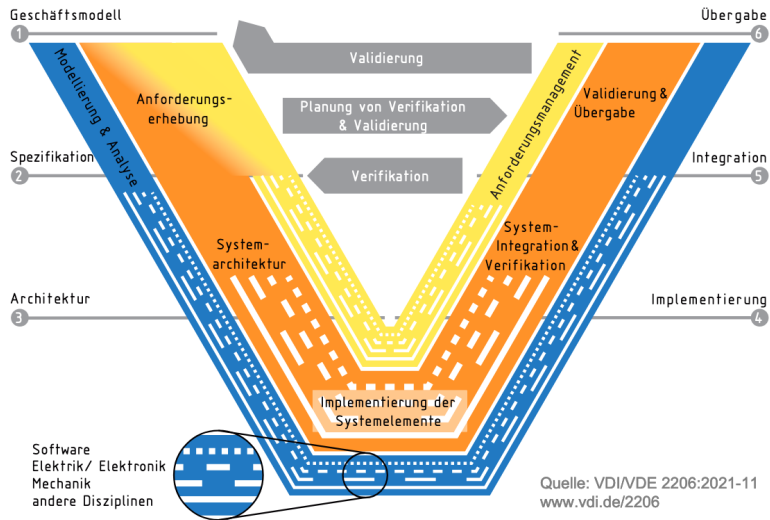
- ▶ Evolution of the waterfall model:
 - ▶ Each phase supported by corresponding verification & validation phase
 - ▶ Feedback between next and previous phase
- ▶ Standard model for public projects in Germany
 - ▶ ... but also a general term for models of this shape.
- ▶ Current: V-Modell XT (“extreme tailoring”)
 - ▶ Shape gives **dependencies**,
 - ▶ **not** necessarily **development timeline**.

Variations of the V-Modell: CIO Bund

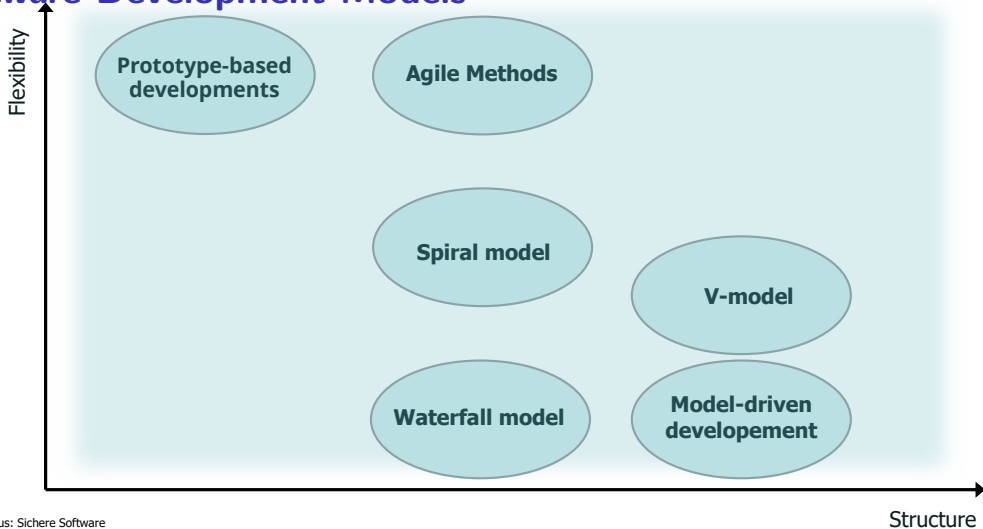


Quelle: <https://www.cio.bund.de/>, Beauftragter der Bundesregierung für IT

Variations of the V-Modell: VDI/VDE



Software Development Models



Quelle S. Paulus: Sichere Software

Development Models for Safety-Critical Systems

Development Models for Critical Systems

- ▶ Ensuring safety/security needs structure.
 - ▶ ... but **too much** structure makes developments bureaucratic, which is **in itself** a safety risk.
 - ▶ Cautionary tale: Ariane-5
- ▶ Standards put emphasis on **process**.
 - ▶ Everything needs to be planned and documented.
 - ▶ Key issues: **auditability**, **accountability**, **traceability**.
- ▶ Best suited development models are **variations of the V-model** or spiral model.
- ▶ A new trend? V-Model XT allows variations of original V-model, e.g.
 - ▶ V-Model for initial developments of a new product,
 - ▶ Agile models (e.g. Scrum) for maintenance and product extensions.

Auditability and Accountability

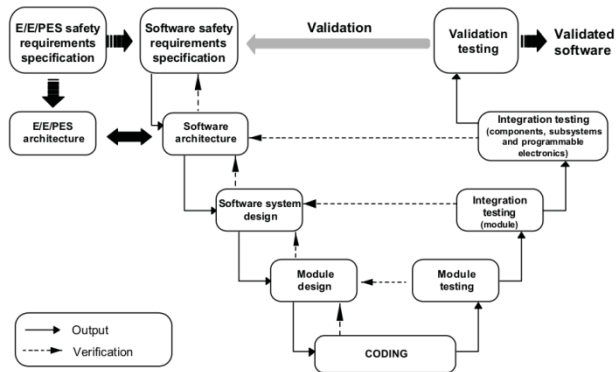
- ▶ **Version control and configuration management** is **mandatory** in safety-critical development (auditability).
- ▶ Keeping track of all artifacts contributing to a particular instance (**build**) of the system (**configuration, baseline**), and their **versions**.
- ▶ **Repository** keeps **all artifacts** in **all versions**.
 - ▶ Centralised (one repository) vs. distributed (every developer keeps own repository)
 - ▶ General model: check out – modify – commit – draw baseline
 - ▶ Baseline: identification of artefacts that are part of the same product release
 - ▶ Concurrency: enforced **lock**, or **merge** after commit.
- ▶ Well-known systems:
 - ▶ Commercial (all outdated): ClearCase, Perforce, Bitkeeper. . .
 - ▶ Open Source: **git** (outdated: svn, cvs, Mercurial)

Traceability

- ▶ The idea of being able to **follow requirements** (in particular, safety requirements) from requirement spec **to the code** (and possibly back).
- ▶ On the simplest level, an Excel sheet with (manual) links to the program.
- ▶ More sophisticated tools (e.g. DOORS):
 - ▶ Decompose requirements, hierarchical requirements
 - ▶ Two-way traceability: from code, test cases, test procedures, and test results back to requirements
 - ▶ e.g. RTCA DO-178C requires that all code is derived from requirements
- ▶ The SysML modelling language has traceability support:
 - ▶ Each model element can be traced to a requirement.
 - ▶ Special associations to express traceability relations.

Development Model in IEC 61508

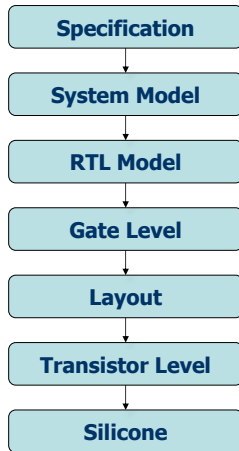
- ▶ IEC 61508 is agnostic with respect to the development model, but:
 - ▶ safety-directed activities are required for each phase of the life cycle (**safety life cycle**).
 - ▶ Development is one part of the life cycle.
- ▶ The only development model mentioned is a V-model:



Development Model in DO-178C

- ▶ DO-178C defines different **processes** in the SW life cycle:
 - ▶ Planning process
 - ▶ Development process, structured in turn into
 - ▶ Requirements process
 - ▶ Design process
 - ▶ Coding process
 - ▶ Integration process
 - ▶ Verification process
 - ▶ Quality assurance process
 - ▶ Configuration management process
 - ▶ Certification liaison process
- ▶ There is no conspicuous diagram, but the Development Process has sub-processes suggesting the phases found in the V-model as well.
 - ▶ Implicit recommendation of the V-model.

Development Model for Hardware



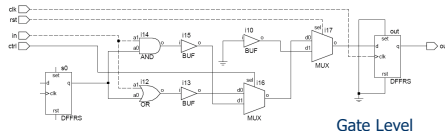
```
SC_MODULE(example) {  
  sc_in_clk clk;  
  sc_in<bool> rst, in, ctrl; sc_out<bool> out;  
  int o, s0;
```

```
  void tick() {  
    if (rst.read()) o = 0;  
    else if (!ctrl.read()) o = s0 | in.read();  
    else o = s0 & in.read();  
    out.write(o); s0 = o;  
  }  
  ...  
}
```

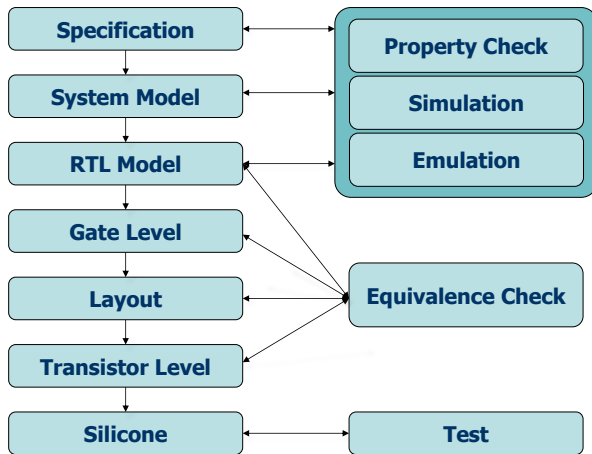
System-Model: SystemC

```
always @(posedge clk)  
  if (rst) out <= 0;  
  else  
    if (!ctrl) out <= s0 | in;  
    else out <= s0 & in;
```

Register-Transfer-Ebene: Verilog



Development Model for Hardware

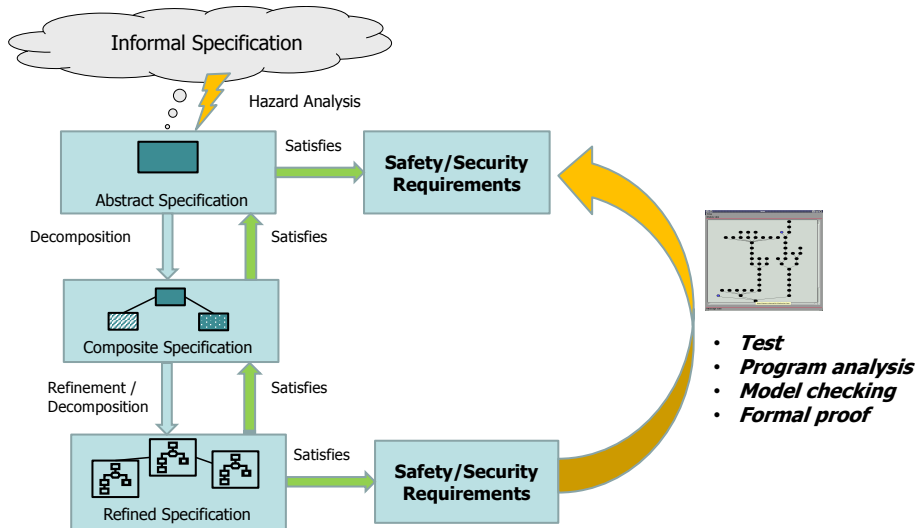


Basic Notions of Formal Software Development

Formal Software Development

- ▶ In a formal development, properties are stated in a rigorous way with a **precise mathematical semantics**.
- ▶ Formal specification requirements can be **proven**.
- ▶ **Advantages** :
 - ▶ Errors can be found early in the development process.
 - ▶ High degree of confidence into the system.
 - ▶ Recommended for high SILs/EALs.
- ▶ **Drawbacks** :
 - ▶ Requires a lot of effort and is thus expensive.
 - ▶ Requires qualified personnel (that would be **you**).
- ▶ There are tools which can help us by
 - ▶ finding (simple) proofs for us (model checkers), or
 - ▶ checking our (more complicated) proofs (theorem provers).

Structuring the Formal Development



Finite State Machines

Finite State Machine (FSM)

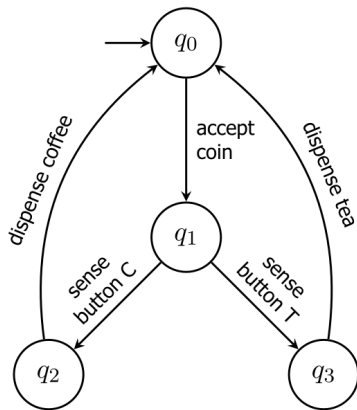
A FSM is given by $\mathcal{M} = \langle \Sigma, \Sigma_0, \rightarrow \rangle$ where

- ▶ Σ is a finite set of **states**,
- ▶ $\Sigma_0 \subseteq \Sigma$ is a set of **initial states**, and
- ▶ $\rightarrow \subseteq \Sigma \times \Sigma$ is a **transition relation**, such that \rightarrow is left-total:

$$\forall s \in \Sigma. \exists s' \in \Sigma. s \rightarrow s'$$

- ▶ The most basic notion of a system.
- ▶ Many variations of this definition exists, e.g. no initial states, state variables or labelled transitions.
- ▶ Note there is no input or output, and no **final** state (key difference to automata).
- ▶ If \rightarrow is a function, the FSM is **deterministic**, otherwise it is **non-deterministic**.

Example: Vending Machine



Transitions:

- 1 Insert/accept coin
- 2 Press/sense button: tea or coffee
- 3 Dispense tea or coffee, return to (1)

$$\mathcal{M} = \langle Q, Q_0, \rightarrow \rangle$$

$$Q = \{q_0, q_1, q_2, q_3\}$$

$$Q_0 = \{q_0\}$$

$$\rightarrow = \{(q_0, q_1), (q_1, q_2), (q_1, q_3), (q_2, q_0), (q_3, q_0)\}$$

Traces

Trace

Given a set Σ of states, a (finite) **trace** is a (finite) sequence $t = \langle t_0, t_1, t_2, \dots, t_n \rangle$ with $t_i \in \Sigma$.

A trace is **admissible** for a FSM $\mathcal{M} = \langle \Sigma, \Sigma_0, \rightarrow \rangle$ iff

- i $t_0 \in \Sigma_0$, and
- ii $\forall i. i < n \implies t_i \rightarrow t_{i+1}$.

- ▶ The empty sequence $\varepsilon = \langle \rangle$ is the empty trace. It is admissible for all FSMs.
- ▶ For a (finite) trace $t = \langle t_i \rangle_{i=0, \dots, n}$, we write $t[i]$ for t_i .
- ▶ The set of all **finite** traces for Σ is written Σ^* ; the set of **infinite** traces is written Σ^ω , and the set of **all** traces is written $\text{Tr}(\Sigma) = \Sigma^* \cup \Sigma^\omega$.

Trace Algebra

- ▶ For a (finite) trace $t = \langle t_i \rangle_{i=0, \dots, n}$, we define the **length** of t as $|t| \stackrel{\text{def}}{=} n + 1$, with $|\varepsilon| = 0$.

Concatenation

Given a (finite) trace s , and a (finite) trace t , their **concatenation** $s \cdot t$ is defined as

$$(s \cdot t)[j] \stackrel{\text{def}}{=} \begin{cases} s[j] & j < |s| \\ t[j - |s|] & j \geq |s| \end{cases}$$

- ▶ Concatenation can be generalised to **sets** of traces, with $S \cdot T \stackrel{\text{def}}{=} \{s \cdot t \mid s \in S, t \in T\}$.

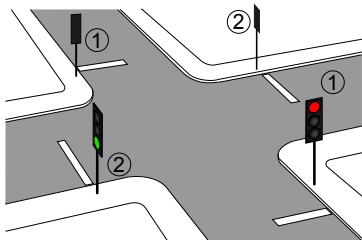
Prefix Ordering

A trace t is a **prefix** of a trace s , written $t \leq s$, iff $\exists t'. t \cdot t' = s$.

- ▶ The prefix ordering generalises to **sets** of traces by $T \leq S$ iff $\forall t. t \in T \implies \exists s. s \in S \wedge t \leq s$.

Example: Street Crossing with Traffic Lights

► States and Transitions:



Source: Wikipedia

$$\mathcal{M} = \langle Q, Q_0, \rightarrow \rangle$$

$$L = \{r, ry, y, g\}$$

$$Q = L \times L$$

$$Q_0 = \{\langle r, g \rangle\}$$

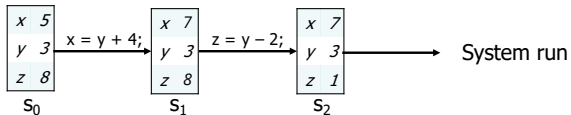
- Do traffic lights switch concurrently or interleaved?
- Each traffic light switches $r \rightarrow ry \rightarrow g \rightarrow y \rightarrow r$
- But not all states should be reachable
- Some states are “bad” (e.g. $\langle g, g \rangle$)

Semantics at Different Levels of Abstraction

- ▶ On an abstract level, the semantics of a **system** (programs running on computers) can be modelled as a FSM.
- ▶ On the **hardware level**, a single computer can be modelled as a FSM:
 - ▶ **State**: Registers, Memory
 - ▶ **Transitions**: read instruction from current PC, execute instruction.
- ▶ On the **software level**, the operational semantics of a program can be modelled as FSM:
 - ▶ **State**: Memory (Variables)
 - ▶ **Transitions**: Effects of each program statement
 - ▶ Different levels of abstraction, depending on programming language

Operational Semantics of Programs

- **States** and transitions between them:



- **Operational semantics** describes relation between states and transitions:

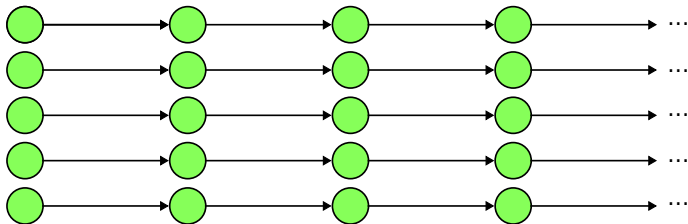
$$\frac{\langle s, e \rangle \rightarrow n}{\langle s, x = e \rangle \rightarrow s[x]^n} \quad \text{hence:} \quad \frac{\langle s_0, y + 4 \rangle \rightarrow 7}{\langle s_0, x = y + 4 \rangle \rightarrow s_1}$$

- **Formal proofs**; e.g. proving

$$\begin{array}{l} x = y + 4; \\ z = y - 2; \end{array} \text{ yields the same final state as } \begin{array}{l} z = y - 2; \\ x = y + 4; \end{array}$$

Semantics of Programs and Requirements

- ▶ Operational semantics gives us the set of all possible system runs:

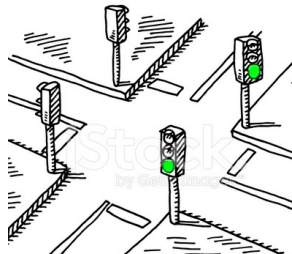


- ▶ We can now consider safety/security-related **requirements**:
 - ▶ Requirements on **single states**,
 - ▶ Requirements on **system runs**,
 - ▶ Requirements on **sets of system runs**.
- ▶ Each gives rise to different **proof methods**.

Requirements on States: Safety Properties

- ▶ Safety property S : *Nothing bad happens.*
 - ▶ i.e. system will never enter a **bad** state.
 - ▶ e.g. lights are never switched to green at the same time.
- ▶ A **bad state**
 - ▶ can be **immediately** recognized;
 - ▶ can **not** be sanitized (by following states).
- ▶ $S \in \mathcal{P}(\Sigma^\omega)$ is a **safety property** iff

$$\forall t. t \notin S \longrightarrow (\exists t_t. t_1 \in \Sigma^* \wedge t_1 \leq t \longrightarrow \forall t_2. t_1 \leq t_2 \longrightarrow t_2 \notin S)$$



Proving Safety Properties

- ▶ In the previous specification, t_1 is **finite**, Hence:
 - ▶ a property is a safety property iff its violation can be detected on a finite trace.
 - ▶ Thus, the **violation** of safety properties can be detected by **testing** (and model-checking).
- ▶ Safety properties are typically proven by **induction**:
 - ▶ Base case: initial states are good.
 - ▶ Step case: each possible transition from a good state leads to a good state.
- ▶ Safety properties can be enforced by **run-time monitors**:
 - ▶ Monitor checks following state in advance, and allows execution only if it is a good state.

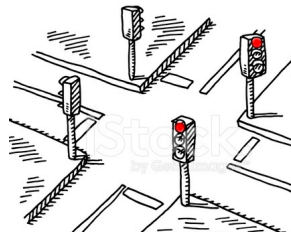
Requirements on Runs: Liveness Properties

- ▶ Liveness property S : *Good things will happen eventually**.
 - ▶ I.e. System will at some point enter a **good** state.
 - ▶ E.g. Traffic lights will eventually go green.
- ▶ A **good state**
 - ▶ is always possible, but
 - ▶ potentially infinite (i.e. no upper bound on when it will occur).
- ▶ $L \in \mathcal{P}(\Sigma^\omega)$ is a **liveness property** iff

$$\forall t. t \in \Sigma^* \implies \exists t_1. t \cdot t_1 \in L$$

- ▶ i.e. all finite traces can be extended to a trace in L .

* NB: *eventually* bedeutet *irgendwann* oder *schlussendlich* aber **nicht** *eventuell*.

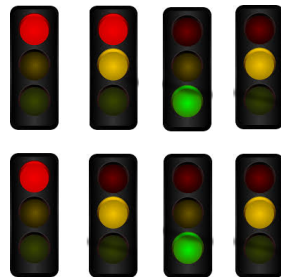


Proving Liveness Properties

- ▶ Liveness properties **cannot** be **enforced** by run-time monitors.
- ▶ Liveness properties **cannot** be checked by **testing**.
- ▶ Liveness properties are typically proven by the help of well-founded orderings:
 - ▶ Define measure function μ on states S : $\mu : S \rightarrow X$ with (X, \preceq) well founded.
 - ▶ Show each transition decreases μ : if $s_1 \rightarrow s_2$ then $\mu(s_2) \preceq \mu(s_1)$
 - ▶ If $\mu(t)$ minimal in \preceq then $t \in S$
- ▶ Example:
 - ▶ Ordering $(X, \preceq) = (\mathbb{N}, \leq)$
 - ▶ Measure denotes the number of transitions until light goes green.

Requirements on Sets of Runs: Safety Hyperproperties

- ▶ Safety hyperproperty S : **System never behaves bad.**
 - ▶ No bad thing happens in a finite set of traces;
 - ▶ (prefixes of) different system runs do not exclude each other;
 - ▶ E.g. Traffic light cycle is always the same.
- ▶ A **bad system** can be recognized by a bad observation (set of finite runs)
 - ▶ A bad observation cannot be sanitized by adding additional runs.
 - ▶ E.g. two system runs having different traffic light cycles.
- ▶ $S \in \mathcal{P}(\mathcal{P}(\Sigma^\omega))$ is a **safety hyperproperty** iff



$$\forall T. T \notin S \longrightarrow (\exists Obs. Obs \in \mathcal{P}_{fin}(\Sigma^*) \wedge Obs \leq T \longrightarrow \forall T'. Obs \leq T' \longrightarrow T' \notin S)$$

(Same as safety property but we talk about sets of traces here!)

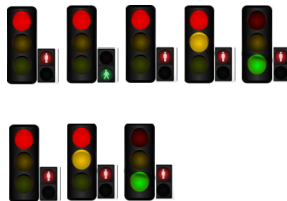
- ▶ Examples: Non-interference

Requirements on Sets of Runs: Liveness Hyperproperties

- ▶ Liveness hyperproperty S : *The system will eventually evolve to a good system.*
 - ▶ Considering any finite part of system behaviour, the system eventually develops into a good system (by extending runs, or adding new runs)
 - ▶ E.g. Green lights for pedestrians can always be omitted.
- ▶ $L \in \mathcal{P}(\mathcal{P}(\Sigma^\omega))$ is a **liveness hyperproperty** iff

$$\forall T. T \in \mathcal{P}(\Sigma^*) \implies \exists G. G \in \mathcal{P}(\Sigma^\omega) \wedge T \leq G \wedge G \in L$$

- ▶ T is a finite set of traces
- ▶ Each observation can be completed to a system G satisfying L
- ▶ Examples: average response time, SLAs, fair scheduling



Facts about (Hyper)Properties

- ▶ Every property is an **intersection** of a **safety** and a **liveness** property.
- ▶ Every hyperproperty is an **intersection** of a **safety** and a **liveness** hyperproperty.

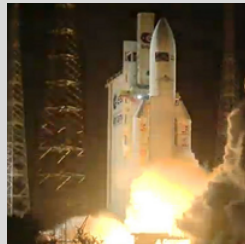
Conclusion & Summary

- ▶ Software development models: structure vs. flexibility
- ▶ Safety standards such as IEC 61508, DO-178C suggest V-model.
 - ▶ Specification and implementation linked by verification and validation.
 - ▶ Variety of artefacts produced at each stage, which have to be subject to external review and audits.
- ▶ Finite state machines are the most basic semantic notion.
- ▶ Requirements are formulated on basis of traces
- ▶ Safety and Security Requirements
 - ▶ Properties: sets of traces, requirements on single states or runs
 - ▶ Safety and Liveness properties
 - ▶ Hyperproperties: sets of properties, requirements on many runs
 - ▶ Safety and Liveness hyperproperties

Systems of High Safety and Security

Lecture 4 from 05.11.2025: Hazard Analysis

Winter term 2025/26

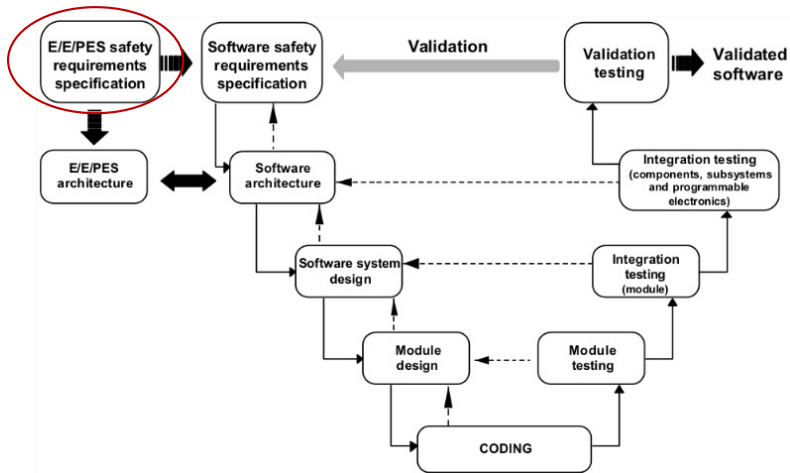


Christoph Lüth

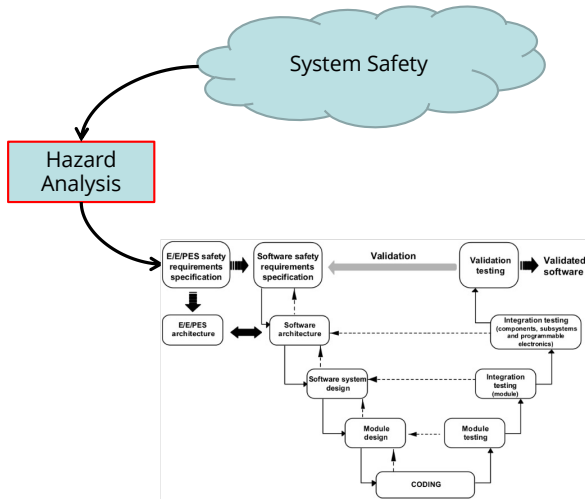
Roadmap

- ▶ Introduction
- ▶ Legal Requirements - Norms and Standards
- ▶ The Development Process
- ▶ Hazard Analysis
- ▶ The Big Picture: Hybrid Systems
- ▶ Temporal Logic with LTL and CTL
- ▶ Operational Semantics
- ▶ Axiomatic Semantics - Specifying Correctness
- ▶ Floyd-Hoare Logic
- ▶ A Simple Compiler and its Correctness
- ▶ Hardware Verification
- ▶ A Simple TinyRV32 Core
- ▶ Conclusions

Hazard Analysis in the Development Cycle



The Purpose of Hazard Analysis



► Hazard Analysis systematically determines a list of **safety requirements**.

► The realization of the safety requirements by the software product must be **verified**.

► The product must be **validated** w.r.t. the safety requirements.

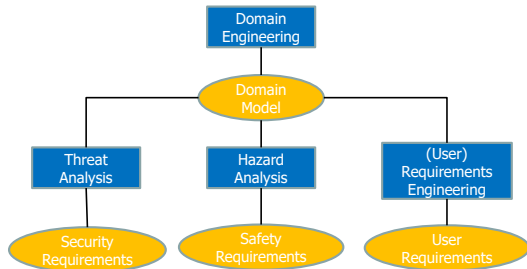
Hazard Analysis ...

- ▶ ... provides the basic **foundations** for **system safety**.
- ▶ ... is performed to **identify** hazards, hazard **effects**, and hazard **causal** factors.
- ▶ ... is used to determine **system risk**, to determine the significance of hazards, and to establish **design measures** that will eliminate or mitigate the identified hazards.
- ▶ ... is used to **systematically** examine systems, subsystems, facilities, components, software, personnel, and their interrelationships.

Clifton Ericson: *Hazard Analysis Techniques for System Safety*.
Wiley-Interscience, 2005.

Side remark: User Requirements

- ▶ The objective of hazard analysis is to produce a **complete** and **consistent** set of safety requirements.
- ▶ Complementary to safety and security requirements, the **user requirements** express what the system should do from the end-user perspective.
- ▶ User requirements are systematically derived in two steps:
 - ▶ **Domain engineering**
 - ▶ **Requirements engineering**



See Bjørner D. (2010) Domain Engineering.

In: Boca P, Bowen J., Siddiqi J. (eds) Formal Methods: State of the Art and New Directions. Springer, London. https://doi.org/10.1007/978-1-84882-736-3_1

Form and Output of Hazard Analysis

The **output** of hazard analysis is a list of **safety requirements** and **documents** detailing how these were derived.

- ▶ Because the process is informal, it can only be **checked** by **reviewing**.
- ▶ It is therefore **critical** that
 - ▶ standard forms of analysis are used,
 - ▶ documents have a standardized form, and
 - ▶ all assumptions are documented.

Classification of Hazard Analysis

- ▶ **Top-down methods** start with an anticipated hazard and work backwards from the hazard event to potential causes for the hazard.
 - ▶ Good for finding causes for hazard;
 - ▶ good for avoiding the investigation of “non-relevant” errors;
 - ▶ bad for detection of missing hazards.
- ▶ **Bottom-up methods** consider “arbitrary” faults and resulting errors of the system and investigate whether they may finally cause a hazard.
 - ▶ Properties are complementary to top-down properties;
 - ▶ Not easy with software where the structure emerges during development.

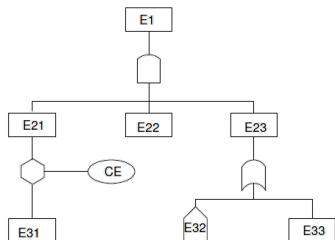
Hazard Analysis Methods

- ▶ **Fault Tree Analysis (FTA)** – top-down
- ▶ **Event Tree Analysis (ETA)** – bottom-up
- ▶ **Failure Modes and Effects Analysis (FMEA)** – bottom up
- ▶ Cause Consequence Analysis – bottom up
- ▶ HAZOP Analysis – bottom up
- ▶ Markov chains in combination with reachability analysis – top-down
 - ▶ Allows for stochastic modelling of complex world models and effective model checking, as long as models are not too large.

Fault Tree Analysis

Fault Tree Analysis (FTA)

- ▶ Top-down deductive failure analysis (of undesired states)
 - ▶ Define undesired top-level event (UE);
 - ▶ Analyze all causes affecting an event to construct fault (sub)tree;
 - ▶ Evaluate fault tree.



FTA: Cut Sets

- ▶ A **cut set** is a set of events that cause the top UE to occur (also called a **fault path**).
- ▶ Cut sets reveal critical and weak links in a system.
- ▶ Extension- **probabilistic** fault trees:
 - ▶ Annotate events with probabilities;
 - ▶ Calculate probabilities for cut sets.
 - ▶ Useful for hardware faults and unpredictable events in the environment.
- ▶ Cut sets can be calculated top down or bottom up.
 - ▶ MOCUS algorithm (Ericson, 2005)
 - ▶ Corresponds to the DNF of underlying formula.
 - ▶ Inhibit gate, priority and gate, exclusive or gate need to be transformed first into AND, OR, with event negation

Fault-Tree Analysis: Process Overview

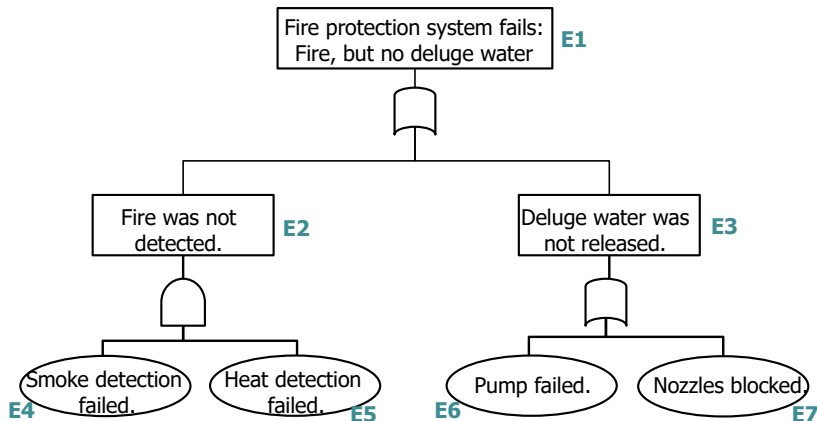
1. Understand system design.
2. For all identified hazards:
 1. Define top undesired event;
 2. Establish boundaries (scope);
 3. Construct fault tree;
 4. Evaluate fault tree (cut sets, probabilities);
 5. Validate fault tree (check if correct and complete);
 6. Modify fault tree (if required);
 7. Document analysis.

MOCUS Algorithm: Calculating the Minimal Cut Sets

1. Name all gates and events.
2. Place top event in the first row.
3. Replace top gate with inputs:
 1. Inputs of AND-gates are kept as lists (sets) in the row;
 2. Inputs of OR-gates are put into a new row each.
4. Move down the fault tree, replacing non-basic events with their inputs this way.
5. When only basic events remain: the remaining lists are the cut sets.
6. Remove all non-minimal cut sets and duplicate cut sets.

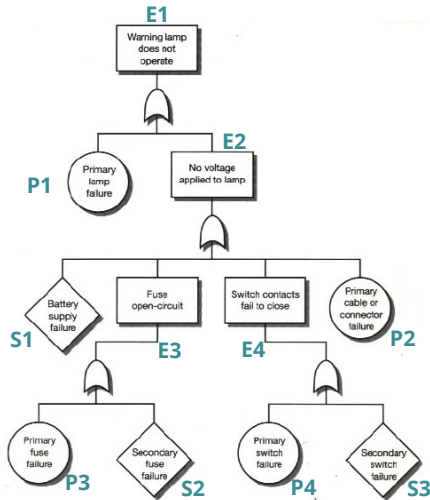
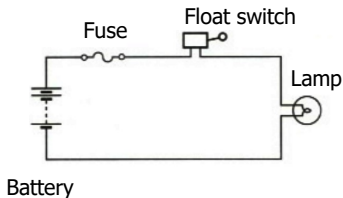
Fault Tree Analysis: First Simple Example

- Consider a simple **fire protection system** connected to smoke/heat detectors.



Fault Tree Analysis: Another Example

- A lamp warning about low level of brake fluid.
- Top undesired event: warning lamp off despite low level of fluid.

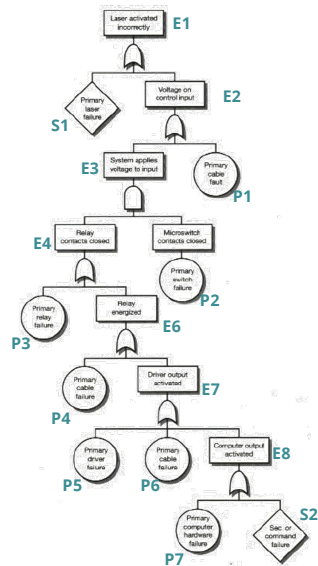
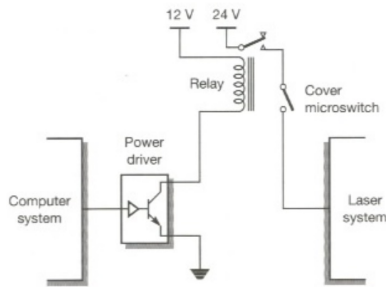


Source: N. Storey, Safety-Critical Computer Systems.

Fault Tree Analysis: Final Example

A laser is operated from a control computer system.

- The laser is connected via a relay and a power driver and protected by a cover switch.
- Top Undesired Event:
Laser activated without explicit command from computer system.



Source: N. Storey, *Safety-Critical Computer Systems*.

Extended FTA: Consider Functional Insufficiencies

► Background

- Whenever functionality based on machine learning is employed, their **actual functional behaviour** may deviate from the **intended functional behaviour**.

► Example

- Deep Neural Networks has been trained to detect obstacles on railway tracks – this function OD is safety critical and needed for autonomous (driverless) trains.
- The **intended functionality** is: OD outputs flag “obstacle is present” if and only if an obstacle on the track exists
- Due to insufficient training of the DNN (the DNN may be implemented correctly!), **the actual functional behaviour** of OD may result in
 - False Negatives: OD signals “no obstacle” though there is one
 - False Positives: OD signals “obstacle” though there is none

Extended FTA: Consider Functional Insufficiencies

- ▶ The standard ISO 21448 has coined the term:
 - ▶ **Safety of the Intended Functionality (SOTIF)** in the context of autonomous road vehicles
 - ▶ A correctly implemented, but insufficiently trained DNN, for example, cannot guarantee the desired SOTIF, though the DNN implementation does not contain any bugs.
- ▶ Consequently, it is advisable to distinguish between different types of events in the nodes of a fault tree
 - ▶ Technical fault or software fault
 - ▶ Functional insufficiency (e.g. due to inadequate training)

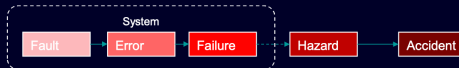
Marc Zeller: **Component Fault and Deficiency Tree (CFDT): Combining Functional Safety and SOTIF Analysis.**
[IMBSA 2022](#): 146-152

Background

Functional Safety & SOTIF

Functional Safety

- ▶ Absence of unacceptable risks (IEC 61508)
- ▶ Risk = combination of hazard probability and severity of the resulting accident
- ▶ Focus: Random hardware faults & systematic software faults



Fault-Error-Failure Chain according to
Avizienis, A., Laprie, J. C., et al. "Basic concepts and taxonomy of dependable
and secure computing", 2004

Safety Of The Intended Functionality (SOTIF)

- ▶ Absence of unreasonable risk due to hazards resulting from functional insufficiencies of the intended functionality or its implementation (ISO 21448)
- ▶ SOTIF activities include the identification of functional insufficiencies and the evaluation of their effects



SOTIF cause and effect model (simplified)

Marc Zeller: **Component Fault and Deficiency Tree (CFDT): Combining Functional Safety and SOTIF Analysis.** [IMBSA 2022](#): 146-152.

FTA - Conclusions

► **Advantages:**

- Structured, rigorous, methodical approach;
- Can be effectively performed and computerized, commercial tool support;
- Easy to learn, do, and follow;
- Combines hardware, software, environment, human interaction.

► **Disadvantages:**

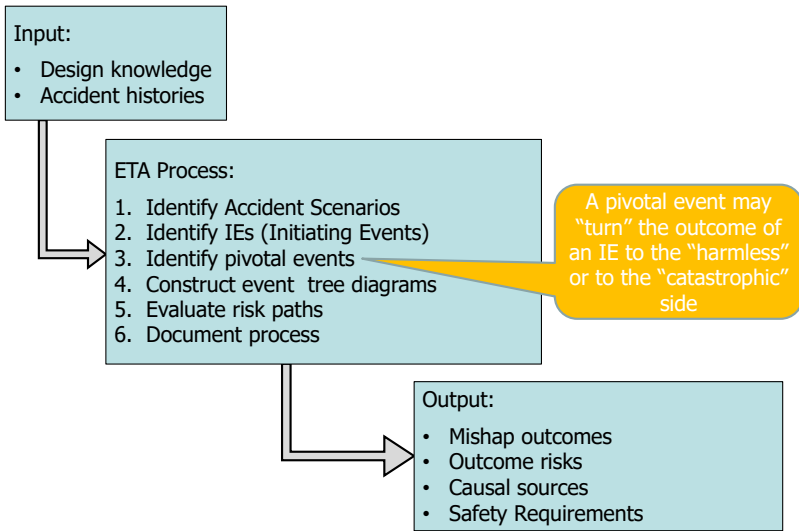
- Can easily become time-consuming and a goal in itself, rather than a tool to identify safety requirements
- Modelling sequential timing and multiple phases is difficult.
- Distinction between events and states always needs to be clarified

Event Tree Analysis

Event Tree Analysis (ETA)

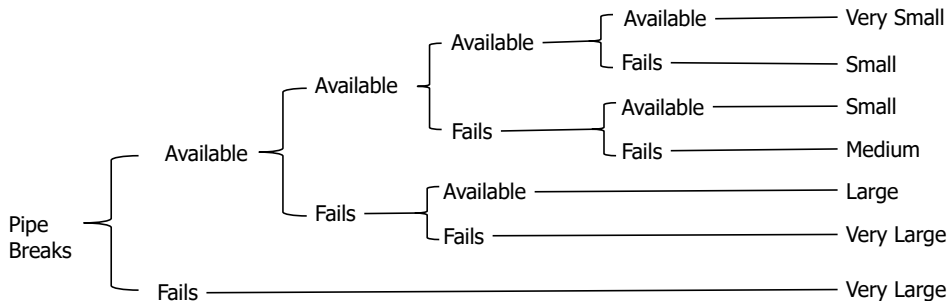
- ▶ Bottom-up method
- ▶ Applies to a chain of cooperating activities
- ▶ Investigates the effect of activities failing while the chain is processed
- ▶ Depicted as binary tree; each node has two leaving edges:
 - ▶ Activity operates correctly
 - ▶ Activity fails
- ▶ Useful for calculating risks by assigning probabilities to edges
- ▶ Complexity: $\mathcal{O}(2^n)$

Event Tree Analysis - Overview



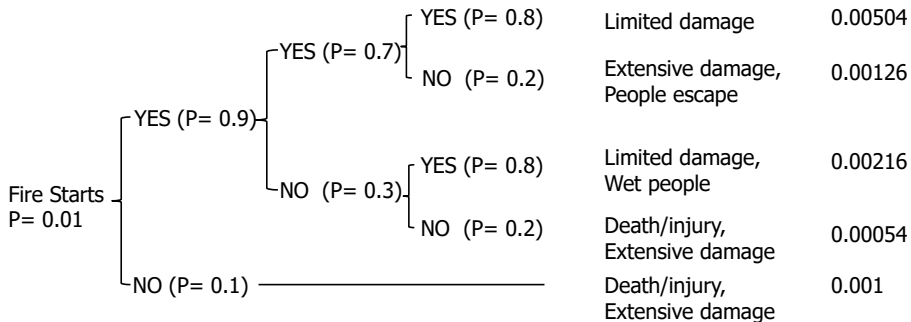
Example: Cooling System for a Nuclear Power Plant

<i>Initiating Event</i>	<i>Pivotal Events</i>				<i>Outcome</i>
	Electricity	Emergency Core Cooling	Fission Product Removal	Containment	Fission Release



Probabilistic ETA: Fire Detection/Suppression System for Office Building

<i>Initiating Event Probability</i>	<i>Pivotal Events</i>			<i>Outcome</i>	<i>Prob.</i>
	Fire Detection Working	Fire Alarms Working	Fire Sprinkler Working		



ETA - Conclusions

► **Advantages:**

- Structured, rigorous and methodical;
- Can be effectively computerized, tool support is available;
- Easy to learn, do, and follow;
- Combines hardware, software, environment and human interaction;
- Can be effectively performed on varying levels of system detail.

► **Disadvantages:**

- An ETA can only have one IE;
- Can overlook subtle system dependencies – pivotal events are not identified;
- Partial success/failure not distinguishable;
- High branching complexity in presence of many pivotal events.

Failure Modes and Effects Analysis

Failure Modes and Effects Analysis (FMEA)

- ▶ Analytic approach to review potential failure modes, their causes, and their effects.
 - ▶ Three approaches: **functional**, **structural** or **hybrid**.
 - ▶ Applicable to hardware and software-related analyses.
 - ▶ It analyzes
 - ▶ the failure mode,
 - ▶ the failure cause,
 - ▶ the failure effect,
 - ▶ its criticality,
 - ▶ and the recommended action,
- and presents them in a **standardized table**.

Software Failure Modes

Guide word	Deviation	Example Interpretation
omission	The system produces no output when it should. Applies to a single instance of a service but may be repeated.	No output in response to change in input; periodic output missing.
commission	The system produces an output, when a perfect system would have produced none. One must consider cases with both, correct and incorrect data.	Same value sent twice in series; spurious output, when inputs have not changed.
early	Output produced before it should be.	Really only applies to periodic events; Output before input is meaningless in most systems.
late	Output produced after it should be.	Excessive latency (end-to-end delay) through the system; late periodic events.
Value (detectable)	Value output is incorrect, but in a way, which can be detected by the recipient.	Out of range.
value (undetectable)	Value output is incorrect, but in a way, which cannot be detected.	Correct in range; but wrong value

Criticality Classes

- Risk as given by the *risk mishap index* (MIL-STD-882):

Severity

1. Catastrophic
2. Critical
3. Marginal
4. Negligible

Probability

- A. Frequent
- B. Probable
- C. Occasional
- D. Remote
- E. Improbable

PROBABILITY LEVELS			
Description	Level	Specific Individual Item	Fleet or Inventory
Frequent	A	Likely to occur often in the life of an item.	Continuously experienced.
Probable	B	Will occur several times in the life of an item.	Will occur frequently.
Occasional	C	Likely to occur sometime in the life of an item.	Will occur several times.
Remote	D	Unlikely, but possible to occur in the life of an item.	Unlikely, but can reasonably be expected to occur.
Improbable	E	So unlikely, it can be assumed occurrence may not be experienced in the life of an item.	Unlikely to occur, but possible.
Eliminated	F	Incapable of occurrence. This level is used when potential hazards are identified and later eliminated.	Incapable of occurrence. This level is used when potential hazards are identified and later eliminated.

SEVERITY CATEGORIES		
Description	Severity Category	Mishap Result Criteria
Catastrophic	1	Could result in one or more of the following: death, permanent total disability, irreversible significant environmental impact, or monetary loss equal to or exceeding \$10M.
Critical	2	Could result in one or more of the following: permanent partial disability, injuries or occupational illness that may result in hospitalization of at least three personnel, reversible significant environmental impact, or monetary loss equal to or exceeding \$1M but less than \$10M.
Marginal	3	Could result in one or more of the following: injury or occupational illness resulting in one or more lost work day(s), reversible moderate environmental impact, or monetary loss equal to or exceeding \$100K but less than \$1M.
Negligible	4	Could result in one or more of the following: injury or occupational illness not resulting in a lost work day, minimal environmental impact, or monetary loss less than \$100K.

Source: MIL-STD-822E, www.system-safety.org/Documents/MIL-STD-882E.pdf

FMEA Example: Airbag Control

- ▶ Consider an **airbag control system**, consisting of
 - ▶ the airbag with gas cartridge;
 - ▶ a control unit with
 - ▶ Output: Release airbag
 - ▶ Input: Accelerometer, impact sensors, seat sensors, ...
- ▶ FMEA:
 - ▶ **Structural**: what can be broken?
 - ▶ Mostly hardware faults.
 - ▶ **Functional**: how can it fail to perform its intended function?
 - ▶ Also applicable for software.

Airbag Control (Structural FMEA)

ID	Mode	Cause	Effect	Crit.	Appraisal
1	Omission	Gas cartridge empty	Airbag not released in emergency	C1	SR-56.3
2	Omission	Cover does not detach	Airbag not released fully in emergency	C1	SR-57.9
3	Omission	Trigger signal not present in emergency.	Airbag not released in emergency	C1	Ref. To SW-FMEA
4	Commission	Trigger signal present in non-emergency	Airbag released during normal vehicle operation	C2	Ref. To SW-FMEA

Airbag Control (Functional FMEA)

ID	Mode	Cause	Effect	Crit.	Appraisal
5-1	Omission	Software terminates abnormally	Airbag not released in emergency.	C1	See 5-1.1, 5-1.2.
5-1.1	Omission	- Division by 0	See 5-1	C1	SR-47.3 Static Analysis
5-1.2	Omission	- Memory fault	See 5-1	C1	SR-47.4 Static Analysis
5-2	Omission	Software does not terminate	Airbag not released in emergency.	C1	SR-47.5 Termination Proof
5-3	Late	Computation takes too long.	Airbag not released in emergency.	C1	SR-47.6 WCET Analysis
5-4	Commission	Spurious signal generated	Airbag released in non-emergency	C2	SR-49.3
5-5	Value (u)	Software computes wrong result	Either of 5-1 or 5-4.	C1	SR-12.1 Formal Verification

FMEA - Conclusions

► Advantages:

- Easily understood and performed;
- Inexpensive to perform, yet meaningful results;
- Provides rigour to focus analysis;
- Tool support available.

► Disadvantages:

- Focuses on single failure modes rather than combination;
- Not designed to identify hazard outside of failure modes;
- Limited examination of human error, external influences or interfaces.

Hazard Analysis as a Reachability Problem

The analysis whether “finally something bad happens” is well-known from **property checking** methods:

- ▶ Create a **world model** describing everything (desired or undesired, with environment, including human users) which might happen in the system under consideration.
- ▶ Specify a logical property P describing the undesired situations.
- ▶ Check the model whether a path – that is, a sequence of state transitions – exists such that P is fulfilled on this path.
- ▶ Calculate the probability that the path fulfilling P is executed (by stochastic model checking, e.g. with PRISM <https://www.prismmodelchecker.org>)
- ▶ Specify as safety requirement that mechanisms shall exist preventing paths leading to P from being taken.

Conclusions

The Seven Principles of Hazard Analysis

Source: Ericson (2005)

- 1) Hazards, mishaps and risk are not chance events.
- 2) Hazards are created during design.
- 3) Hazards are comprised of three components (HE, IM, T/T).
- 4) Hazards and mishap risk is the core safety process.
- 5) Hazard analysis is the key element of hazard and mishap risk management.
- 6) Hazard management involves seven key hazard analysis types.
- 7) Hazard analysis primarily encompasses seven hazard analysis techniques.

Summary

- ▶ Hazard Analysis is the **start** of the formal development.
- ▶ Its most important output are **safety requirements**.
- ▶ Adherence to safety requirements has to be **verified** during development and **validated** at the end.
- ▶ We distinguish different types of analysis:
 - ▶ Top-Down analysis (Fault Trees)
 - ▶ Bottom-up (FMEAs, Event Trees)
- ▶ It makes sense to **combine** different types of analyses, as their results are complementary.

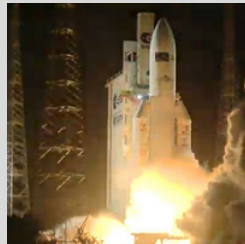
Conclusions

- ▶ Hazard Analysis is a creative process, as it takes an informal input („system safety“) and produces a formal output (safety requirements).
- ▶ Its results cannot be formally proven, merely checked and reviewed.
- ▶ Review plays a key role.
- ▶ Therefore,
 - ▶ documents must be readable, understandable, auditable;
 - ▶ analysis must be in well-defined and well-documented format;
 - ▶ all assumptions must be well documented.

Systems of High Safety and Security

Lecture 6 from 19.11.2025: Temporal Logic with LTL and CTL

Winter term 2025/26



Christoph Lüth

Roadmap

- ▶ Introduction
- ▶ Legal Requirements - Norms and Standards
- ▶ The Development Process
- ▶ Hazard Analysis
- ▶ The Big Picture: Hybrid Systems
- ▶ Temporal Logic with LTL and CTL
- ▶ Operational Semantics
- ▶ Axiomatic Semantics - Specifying Correctness
- ▶ Floyd-Hoare Logic
- ▶ A Simple Compiler and its Correctness
- ▶ Hardware Verification
- ▶ A Simple TinyRV32 Core
- ▶ Conclusions

Introduction

- ▶ We have seen that **state machines** are a general system model.
- ▶ Now the question is: how do we state and **prove** properties of systems modelled as finite state machines?
- ▶ There are many answers, depending on the level of **abstraction**. On the most abstract level, we can use **temporal logic**.
- ▶ On this abstract level, the question is how to prove a property ϕ of a system modelled as a FSM \mathcal{M} .

The Model-Checking Problem

The Basic Question

Given a model \mathcal{M} , and a property ϕ , we want to know whether

$$\mathcal{M} \models \phi$$

- ▶ What is \mathcal{M} ?
- ▶ What is ϕ ?
- ▶ How to prove it?

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- ▶ How to prove it? Enumerating states — **model checking**

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- ▶ What is \mathcal{M} ? **Finite state machines**
- ▶ What is ϕ ? **Temporal logic**
- ▶ How to prove it? Enumerating states — **model checking**
 - ▶ The basic **problem**: **state explosion**

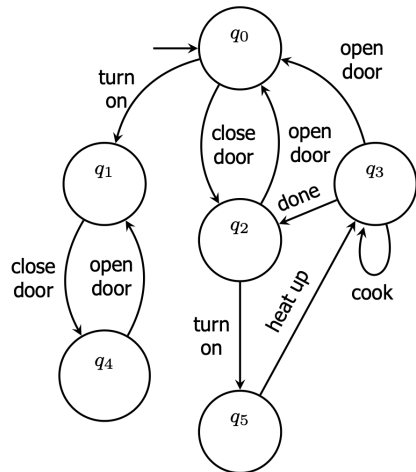
Example: A Simple Baking Oven

- ▶ The oven has states and operations:
 - ▶ open and close door,
 - ▶ turn oven on and off,
 - ▶ warm up and cook.
- ▶ How do they interact?



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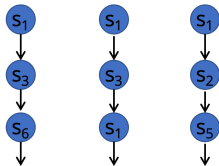
Questions to Ask

- ▶ We want to answer **questions** about the system **behaviour** like
 - ▶ Can the cooker heat up with the door open?
 - ▶ When the start button is pushed, will the cooker eventually heat up?
 - ▶ When the cooker is correctly started, will the cooker eventually heat up?
 - ▶ When an error occurs, will it be still possible to cook?
- ▶ We are interested in questions on the evolution of the system over time, i.e. possible **traces** of the system given by a succession of states.
- ▶ The tool to formalize and answer these questions is **temporal logic**.

Basic Concepts of Time

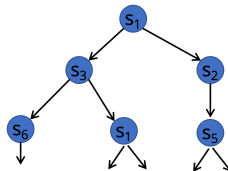
Linear Time

- ▶ Every moment has a **unique** successor
- ▶ Infinite **sequences** of moments
- ▶ Linear Temporal Logic (LTL)



Branching Time

- ▶ Every moment has **several** successors
- ▶ Infinite **tree** of moments
- ▶ Computational Tree Logic (CTL)



Atomic Propositions and States

- ▶ The basis of temporal logics are FSMs and **state predicates**.
- ▶ At each state of an FSM, a set of state predicates hold.
- ▶ This is called a **Kripke structure**.

Definition: Kripke Structure

For a set $Prop$ of atomic propositions, a **Kripke structure** $\mathcal{K} = \langle \mathcal{M}, V \rangle$ is given by a FSM $\mathcal{M} = \langle Q, Q_0, \rightarrow \rangle$ and a function $V : Q \rightarrow 2^{Prop}$ mapping each state to the set of atomic propositions holding in that state.

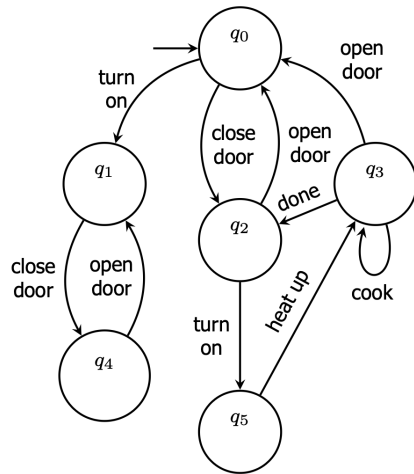
For $q \in Q, p \in Prop$, we write $q \models p$ if $p \in V(q)$ (p holds in q).

Example: The Simple Baking Oven

- ▶ Atomic propositions:

- ▶ C : door closed.
- ▶ S : oven started
- ▶ H : oven hot
- ▶ E : error occurred

- ▶ Label states appropriately

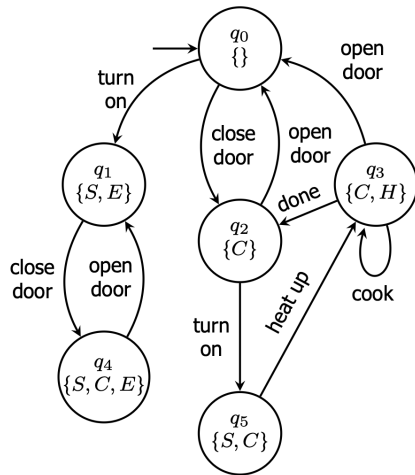


Example: The Simple Baking Oven

► Atomic propositions:

- C : door closed.
- S : oven started
- H : oven hot
- E : error occurred

► Label states appropriately



Linear Temporal Logic (LTL)

$\phi ::=$	$\top \mid \perp \mid a$	— True, false, atomic
	$\neg\phi \mid \phi_1 \wedge \phi_2 \mid \phi_1 \vee \phi_2 \mid \phi_1 \longrightarrow \phi_2$	— Propositional formulae
	$X\phi$	— Next state
	$\Diamond\phi$	— Some Future State
	$\Box\phi$	— All future states (Globally)
	$\phi_1 U \phi_2$	— Until

- ▶ Operator precedence: Unary operators; then U ; then \wedge, \vee ; then \longrightarrow .
- ▶ An atomic formula p above denotes a **state predicate**.
- ▶ From these, we can define other operators, such as $\phi R \psi$ (release) or $\phi W \psi$ (weak until).

Satisfaction and Models of LTL

Given a path (infinite trace) p and an LTL formula ϕ , the **satisfaction relation** $p \models \phi$ is defined inductively as follows:

$$p \models \text{true}$$

$$p \not\models \text{false}$$

$$p \models a \text{ iff } p[0] \models a$$

$$p \models \neg\phi \text{ iff } p \not\models \phi$$

$$p \models \phi \wedge \psi \text{ iff } p \models \phi \text{ and } p \models \psi$$

$$p \models \phi \vee \psi \text{ iff } p \models \phi \text{ or } p \models \psi$$

$$p \models \phi \longrightarrow \psi \text{ iff whenever } p \models \phi \text{ then } p \models \psi$$

$$p \models X\phi \text{ iff } p^1 \models \phi$$

$$p \models \Box\phi \text{ iff for all } i, \text{ we have } p^i \models \phi$$

$$p \models \Diamond\phi \text{ iff there is } i \text{ such that } p^i \models \phi$$

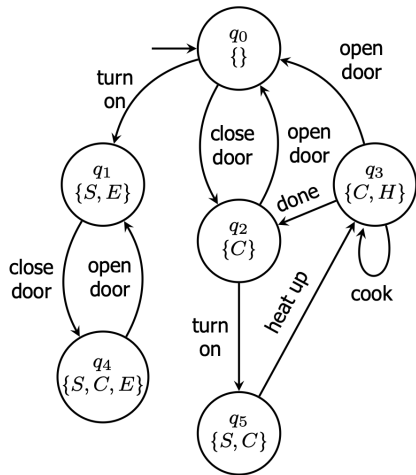
$$p \models \phi U \psi \text{ iff there is } i \text{ } p^i \models \psi \text{ and for all } j = 1, \dots, i-1, \text{ } p^j \models \phi$$

Models of LTL formulae

A Kripke structure $\mathcal{K} = \langle M, V \rangle$ satisfies an LTL formula ϕ , $\mathcal{K} \models \phi$, iff for every path $p \in \text{Tr}(\mathcal{M})$, $p \models \phi$.

Example: The Simple Baking Oven

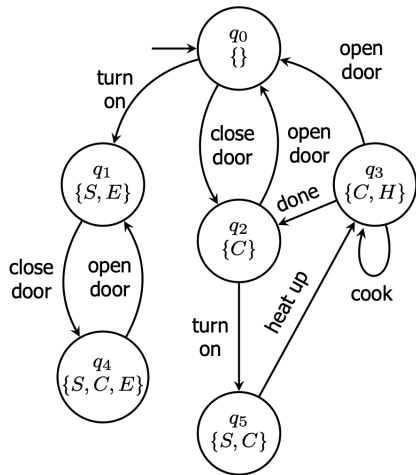
- If the cooker heats, then is the door closed?



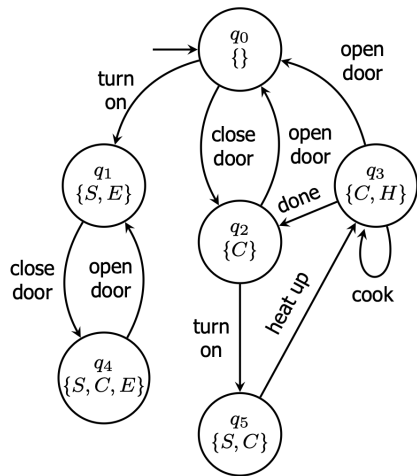
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- If the cooker heats, then is the door closed?

$$\Box H \longrightarrow C$$



Example: The Simple Baking Oven

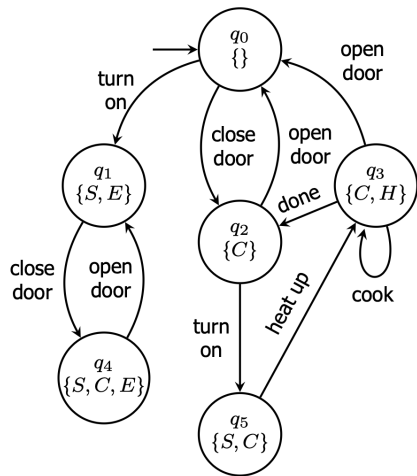


- If the cooker heats, then is the door closed?

$$\Box H \longrightarrow C \quad \checkmark$$

- Is it always possible to recover from an error?

Example: The Simple Baking Oven



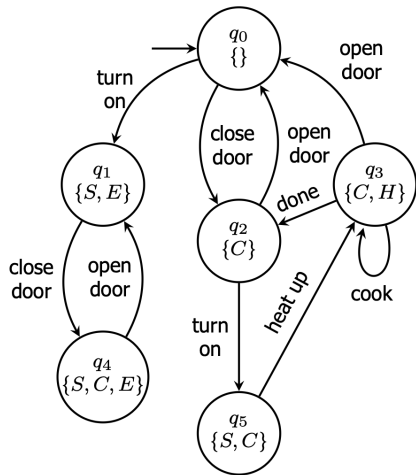
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$$\Box(E \longrightarrow \Diamond(\neg E))$$

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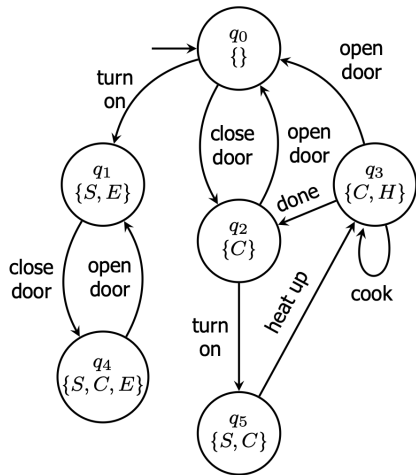
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- Need to add a reset transition.
- Is it always possible to heat up, then cook?

Example: The Simple Baking Oven



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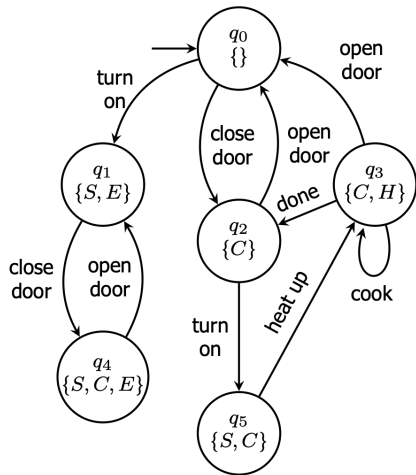
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$$\Diamond(S \longrightarrow X H)$$

Example: The Simple Baking Oven



- ▶ If the cooker heats, then is the door closed?

$$\Box H \longrightarrow C \quad \checkmark$$

- ▶ Is it always possible to recover from an error?

$$\Box(E \longrightarrow \Diamond(\neg E)) \quad \times$$

- ▶ Need to add a reset transition.

- ▶ Is it always possible to heat up, then cook?

$$\Diamond(S \longrightarrow X H) \quad \times$$

- ▶ Always possible to avoid cooking.
- ▶ Cannot express 'there are paths in which we can always cook'.

Computational Tree Logic (CTL)

- ▶ LTL does not allow us to quantify over paths, e.g. assert the existence of a path satisfying a particular property.
- ▶ To a limited degree, we can solve this problem by negation: instead of asserting a property ϕ , we check whether $\neg\phi$ is satisfied; if that is not the case, ϕ holds. But this does not work for mixtures of universal and existential quantifiers.
- ▶ Computational Tree Logic (CTL) is an extension of LTL which allows this by adding universal and existential quantifiers to the modal operators.
- ▶ The name comes from considering paths in the **computational tree** obtained by **unwinding** the FSM.

CTL Formulae

$\phi ::= \top \mid \perp \mid p$
| $\neg\phi \mid \phi_1 \wedge \phi_2 \mid \phi_1 \vee \phi_2 \mid \phi_1 \longrightarrow \phi_2$
| $AX\phi \mid EX\phi$
| $AF\phi \mid EF\phi$
| $AG\phi \mid EG\phi$
| $A[\phi_1 \ U \ \phi_2] \mid E[\phi_1 \ U \ \phi_2]$

- True, false, atomic
- Propositional formulae
- All or some next state
- All or some future states
- All or some global future
- Until all or some

Satisfaction

- ▶ Note that CTL formulae can be considered to be a LTL formulae with a 'modality' (A or E) added on top of each temporal operator.
- ▶ Generally speaking, the A modality says the temporal operator holds for all paths, and the E modality says the temporal operator only holds for all least one path.
- ▶ Of course, that strictly speaking is not true, because the arguments of the temporal operators are in turn CTL formulae, so we need recursion.
- ▶ This all explains why we do not define a satisfaction for a single path p , but satisfaction with respect to a specific **state** in an FSM.

Satisfaction for CTL

Given a Kripke-structure $\mathcal{K} = \langle \mathcal{M}, V \rangle$, $s \in \Sigma$ and a CTL formula ϕ , then $\mathcal{K}, s \models \phi$ is defined inductively as follows:

$$\mathcal{K}, s \models \text{true}$$

$$\mathcal{K}, s \not\models \text{false}$$

$$\mathcal{K}, s \models p \text{ iff } s \models p$$

$$\mathcal{K}, s \models \phi \wedge \psi \text{ iff } \mathcal{K}, s \models \phi \text{ and } \mathcal{K}, s \models \psi$$

$$\mathcal{K}, s \models \phi \vee \psi \text{ iff } \mathcal{K}, s \models \phi \text{ or } \mathcal{K}, s \models \psi$$

$$\mathcal{K}, s \models \phi \longrightarrow \psi \text{ iff whenever } \mathcal{K}, s \models \phi \text{ then } \mathcal{K}, s \models \psi$$

...

Satisfaction for CTL (c'ed)

Given a Kripke-structure $\mathcal{K} = \langle \mathcal{M}, V \rangle$, $s \in \Sigma$ and a CTL formula ϕ , then $\mathcal{K}, s \models \phi$ is defined inductively as follows:

...

$\mathcal{K}, s \models \text{AX } \phi$ iff for all s_1 with $s \rightarrow s_1$, we have $\mathcal{K}, s_1 \models \phi$

$\mathcal{K}, s \models \text{EX } \phi$ iff for some s_1 with $s \rightarrow s_1$, we have $\mathcal{K}, s_1 \models \phi$

Satisfaction for CTL (c'ed)

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$\mathcal{K}, s \models \text{AG } \phi$ iff for all paths p with $p[0] = s$, we have $\mathcal{K}, p[i] \models \phi$ for all $i \geq 1$

$\mathcal{K}, s \models \text{EG } \phi$ iff there is a path p with $p[0] = s$ and $\mathcal{K}, p[i] \models \phi$ for all $i \geq 1$

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$\mathcal{K}, s \models \text{AF } \phi$ iff for all paths p with $p[0] = s$, we have $\mathcal{K}, p[i] \models \phi$ for some i

$\mathcal{K}, s \models \text{EF } \phi$ iff there is a path p with $p[0] = s$ and $\mathcal{K}, p[i] \models \phi$ for some i

Satisfaction for CTL (c'ed)

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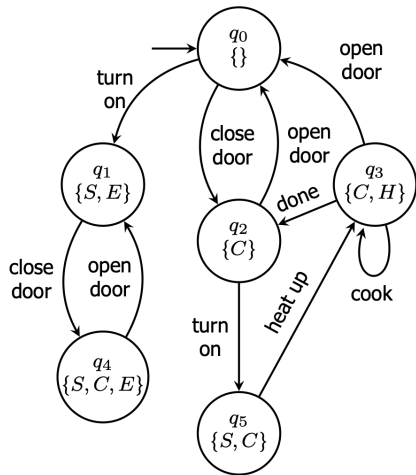
$\mathcal{K}, s \models \text{EF } \phi$ iff there is a path p with $p[0] = s$ and $\mathcal{K}, p[i] \models \phi$ for some i

$\mathcal{K}, s \models \text{A}[\phi \text{ U } \psi]$ iff for all paths p with $p[0] = s$, there is i
with $\mathcal{K}, p[i] \models \psi$ and for all $j < i$, $\mathcal{K}, p[j] \models \phi$

$\mathcal{K}, s \models \text{E}[\phi \text{ U } \psi]$ iff there is a path p with $p_1 = s$ and there is i
with $\mathcal{K}, p[i] \models \psi$ and for all $j < i$, $\mathcal{K}, p[j] \models \phi$

Example: The Simple Baking Oven

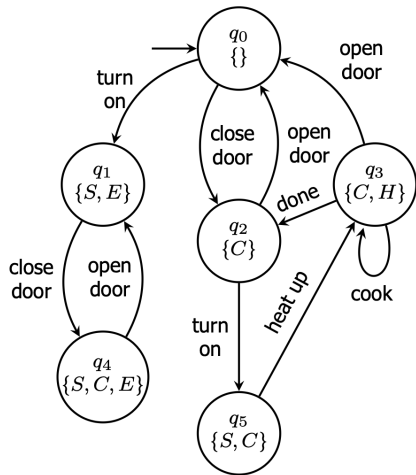
- Whenever the oven is hot, the door is closed.



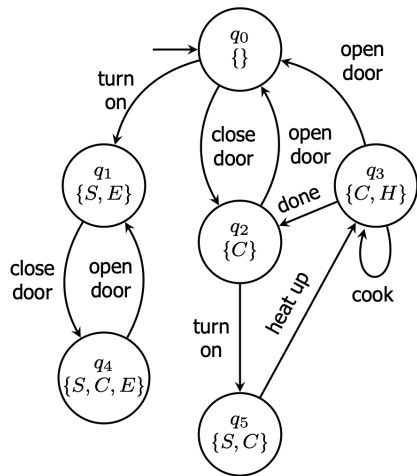
Example: The Simple Baking Oven

- Whenever the oven is hot, the door is closed.

$$AG H \longrightarrow C$$



Example: The Simple Baking Oven

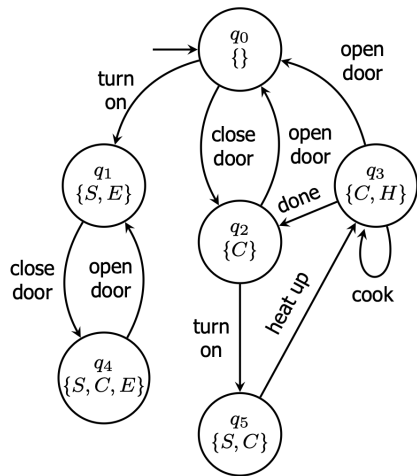


- ▶ Whenever the oven is hot, the door is closed.

$$AG H \longrightarrow C \quad \checkmark$$

- ▶ After cooking, we will get access to the food:

Example: The Simple Baking Oven



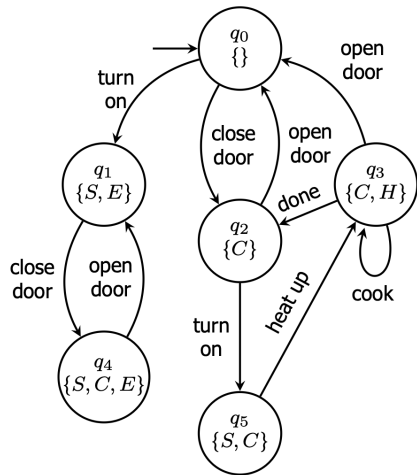
- ▶ Whenever the oven is hot, the door is closed.

$$AG H \longrightarrow C \quad \checkmark$$

- ▶ After cooking, we will get access to the food:

$$AF(H \longrightarrow AF \neg C)$$

Example: The Simple Baking Oven



- ▶ Whenever the oven is hot, the door is closed.

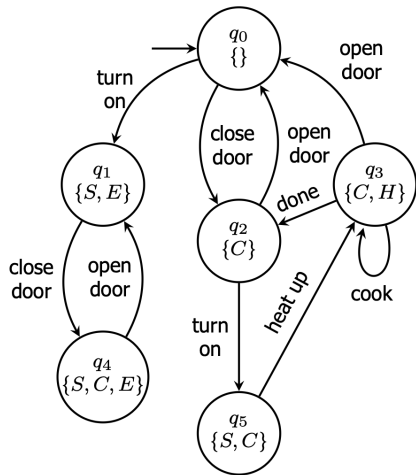
$$AG H \longrightarrow C \quad \checkmark$$

- ▶ After cooking, we will get access to the food:

$$AF(H \longrightarrow AF \neg C) \quad \times$$

- ▶ After cooking, we may get access to the food:

Example: The Simple Baking Oven



- ▶ Whenever the oven is hot, the door is closed.

$$AG H \longrightarrow C \quad \checkmark$$

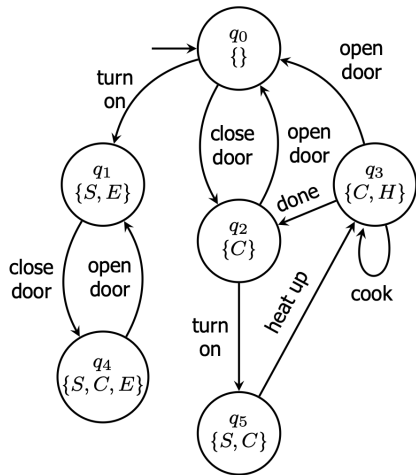
- ▶ After cooking, we will get access to the food:

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- ▶ After cooking, we may get access to the food:

$$AF(H \longrightarrow EF \neg C)$$

Example: The Simple Baking Oven



- Whenever the oven is hot, the door is closed.

$$AG H \longrightarrow C \quad \checkmark$$

- After cooking, we will get access to the food:

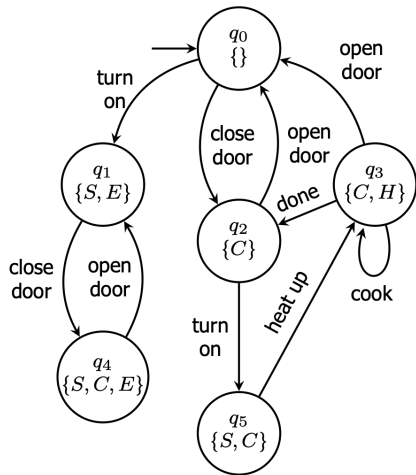
$$AF(H \longrightarrow AF \neg C) \quad \times$$

- After cooking, we may get access to the food:

$$AF(H \longrightarrow EF \neg C) \quad \times$$

- The oven will always eventually heat up

Example: The Simple Baking Oven



- Whenever the oven is hot, the door is closed.

$$AG H \longrightarrow C \quad \checkmark$$

- After cooking, we will get access to the food:

$$AF(H \longrightarrow AF \neg C) \quad \times$$

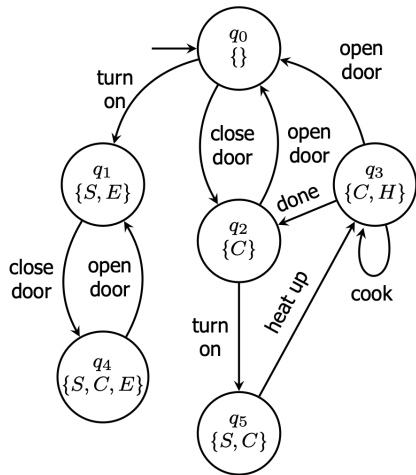
- After cooking, we may get access to the food:

$$AF(H \longrightarrow EF \neg C) \quad \times$$

- The oven will always eventually heat up

$$AG(EF(\neg H \wedge EX H))$$

Example: The Simple Baking Oven



- ▶ Whenever the oven is hot, the door is closed.

$$AG H \longrightarrow C \quad \checkmark$$

- ▶ After cooking, we will get access to the food:

$$AF(H \longrightarrow AF \neg C) \quad \times$$

- ▶ After cooking, we may get access to the food:

$$AF(H \longrightarrow EF \neg C) \quad \times$$

- ▶ The oven will always eventually heat up

$$AG(EF(\neg H \wedge EX H)) \quad \times$$

- ▶ Only with reset transition.

Patterns of Specification

- ▶ Something bad (p) cannot happen: $AG \neg p$
- ▶ p occurs infinitely often: $AG(AF p)$
- ▶ p occurs eventually: $AF p$
- ▶ In the future, p will hold eventually forever: $AF AG p$
- ▶ Whenever p will hold in the future, q will hold eventually: $AG(p \longrightarrow AF q)$
- ▶ In all states, p is always possible: $AG(EF p)$

LTL and CTL

- ▶ We have seen that CTL is more expressive than LTL, but (surprisingly), there are properties which we can formalise in LTL but not in CTL!
- ▶ Example: all paths which have a p along them also have a q along them.
- ▶ LTL: $\Diamond p \longrightarrow \Diamond q$
- ▶ CTL: **Not** $\text{AF } p \longrightarrow \text{AF } q$ (would mean: if all paths have p , then all paths have q), neither $\text{AG}(p \longrightarrow \text{AF } q)$ (which means: if there is a p , it will be followed by a q).
- ▶ The logic CTL^* combines both LTL and CTL (but we will not consider it further here).

State Explosion and Complexity

- ▶ The basic problem of model checking is **state explosion**.
- ▶ State grows **exponentially**: n states have a state space of 2^n . Add one integer variable with $n = 2^{32}$ states, and this gets intractable.
- ▶ Theoretically, there is not much hope. The basic problem of deciding whether a particular formula holds is known as the satisfiability problem, and for the temporal logics we have seen, its complexity is as follows:
 - ▶ LTL without U is *NP*-complete.
 - ▶ LTL is *PSPACE*-complete.
 - ▶ CTL is *EXPTIME*-complete.
- ▶ The good news is that at least it is **decidable**. Practically, **state abstraction** is the key technique. E.g. instead of considering all possible integer values, consider only whether i is zero or larger than zero.

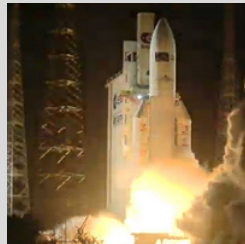
Summary

- ▶ Model-checking allows us to show to show properties of systems by enumerating the system's states, by modelling systems as **finite state machines**, and expressing properties in temporal logic.
- ▶ We considered Linear Temporal Logic (LTL) and Computational Tree Logic (CTL). LTL allows us to express properties of single paths, CTL allows quantifications over all possible paths of an FSM.
- ▶ The basic problem: the system state can quickly get **huge**, and the basic complexity of the problem is **horrendous**. Use of abstraction and state compression techniques make model-checking bearable.
- ▶ Next: what has software to do with all of this? Operational Semantics.

Systems of High Safety and Security

Lecture 7 from 26.11.2025: Operational Semantics

Winter term 2025/26



Christoph Lüth

Roadmap

- ▶ Introduction
- ▶ Legal Requirements - Norms and Standards
- ▶ The Development Process
- ▶ Hazard Analysis
- ▶ The Big Picture: Hybrid Systems
- ▶ Temporal Logic with LTL and CTL
- ▶ Operational Semantics
- ▶ Axiomatic Semantics - Specifying Correctness
- ▶ Floyd-Hoare Logic
- ▶ A Simple Compiler and its Correctness
- ▶ Hardware Verification
- ▶ A Simple TinyRV32 Core
- ▶ Conclusions

Semantics — what and why?

Semantics (noun [uncountable]) 2. the meaning of words, phrases or systems

— Oxford Learner's Dictionaries

Describes the meaning of a program in mathematical precise and unambiguous way:

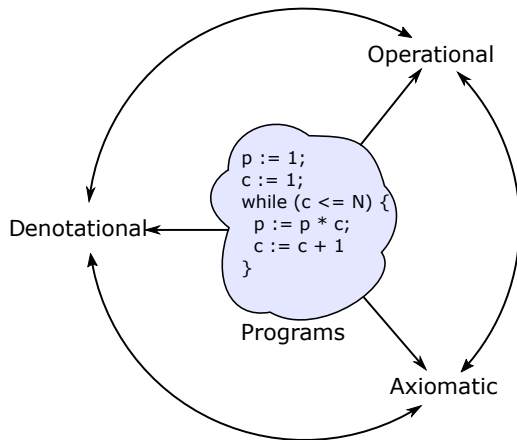
- ▶ Better compilers — independent of a particular compiler implementation.
- ▶ We will know when it should produce a result or not, and which situations to avoid.
- ▶ Lets us reason about program and compiler correctness.

Semantics of Programming Languages

Historically, there are three ways to write down the semantics of a programming language:

- ▶ **Operational semantics** describes the meaning of programs by specifying how they **executes** on an abstract machine.
- ▶ **Denotational semantics** assigns a **meaning** to programs: a partial function on the system state.
- ▶ **Axiomatic semantics** gives a meaning to programs by giving proof rules. A prominent example of this is the Floyd-Hoare logic.

A Tale of Three Semantics



- ▶ Each semantics is a view of the program.
- ▶ All semantics should be equivalent.
- ▶ In particular, for axiomatic semantics (Floyd-Hoare logic), rules should be correct.

Our Wee Language

- ▶ We consider a **simple imperative language** (like C or Java).
- ▶ It has only integer types (no arrays, structs, pointers or references), no function calls, and no local variables.
- ▶ It is **Turing-complete** (we can write all programs).
- ▶ We give the programs in terms of an **abstract syntax**.

Expressions

Expressions

- ▶ Our simple language has the following expressions:

$$\begin{aligned} e ::= \mathbb{Z} \mid \mathbf{ldt} \mid \mathit{true} \mid \mathit{false} \\ \mid e_1 + e_2 \mid e_1 - e_2 \mid e_1 * e_2 \mid e_1 / e_2 \\ \mid e_1 == e_2 \mid e_1 < e_2 \\ \mid !e \mid e_1 \&\& e_2 \mid e_1 || e_2 \end{aligned}$$

- ▶ This **abstract** (not concrete) syntax, it lacks parentheses and precedence etc.
- ▶ Expressions (terms) are represented as **trees**.

Structural Operational Semantics

- ▶ Defined inductively by **rules** of the form

$$\frac{\langle t', a' \rangle \rightarrow b' \quad \phi(a', t, t')}{\langle t, a \rangle \rightarrow b}$$

- ▶ t is a tree of depth 1 (one top symbol, all children are distinct variables)
- ▶ a is input data (e.g. the state), b return data (e.g. a value)
- ▶ Applying the rule corresponds to a **state transition** of the abstract machine

States

- ▶ States are **finite partial maps** represented by **right-unique** relations

$$f : X \rightarrow A \subseteq X \times A \text{ such that } \forall x, a, b. (x, a) \in f \wedge (x, b) \in f \implies a = b$$

- ▶ State for our language: $\Sigma \stackrel{\text{def}}{=} \mathbf{Idt} \rightarrow \mathbb{Z}$ (identifiers mapped to integers)

- ▶ Notation:

- ▶ $\langle x \mapsto 5, y \mapsto 7, z \mapsto 10 \rangle$ für $\{(x, 5), (y, 7), (z, 10)\}$
- ▶ $f(x)$ for the value of x in f (*lookup*)
- ▶ $f(x) = \perp$ if x not in f (*undefined*) and $\text{def}(f(x))$ für $(x, y) \in f$ (*defined*)
- ▶ $f \setminus x$ to **remove** x from f
- ▶ $f[x \mapsto n]$ to **update** f at x with the value n .

Rules of the Operational Semantics

- ▶ An expression e with a state σ evaluates to an integer $n \in \mathbb{Z}$ or a boolean $b \in \mathbb{B}$:

$$e ::= \mathbb{Z} \mid \mathbf{ldt} \mid \mathit{true} \mid \mathit{false} \mid \dots \quad \langle e, \sigma \rangle \rightarrow_{Exp} n \mid b$$

- ▶ **Rules:**

$$\frac{i \in \mathbb{Z}}{\langle i, \sigma \rangle \rightarrow_{Exp} i}$$

$$\frac{b \in \mathbb{B}}{\langle b, \sigma \rangle \rightarrow_{Exp} b}$$

$$\frac{x \in \mathbf{ldt}, x \in \text{dom}(\sigma), \sigma(x) = v}{\langle x, \sigma \rangle \rightarrow_{Exp} v}$$

Operational Semantics: Arithmetic Expressions

► Expressions:

$$e ::= \dots \mid e_1 + e_2 \mid e_1 - e_2 \mid e_1 * e_2 \mid e_1 / e_2 \mid \dots \quad \langle e, \sigma \rangle \rightarrow_{Exp} n$$

► Rules:

$$\frac{\langle e_1, \sigma \rangle \rightarrow_{Exp} n_1 \quad \langle e_2, \sigma \rangle \rightarrow_{Exp} n_2 \quad n_i \in \mathbb{Z}}{\langle e_1 + e_2, \sigma \rangle \rightarrow_{Exp} n_1 + n_2}$$

$$\frac{\langle e_1, \sigma \rangle \rightarrow_{Exp} n_1 \quad \langle e_2, \sigma \rangle \rightarrow_{Exp} n_2 \quad n_i \in \mathbb{Z}}{\langle e_1 - e_2, \sigma \rangle \rightarrow_{Exp} n_1 - n_2}$$

$$\frac{\langle e_1, \sigma \rangle \rightarrow_{Exp} n_1 \quad \langle e_2, \sigma \rangle \rightarrow_{Exp} n_2 \quad n_i \in \mathbb{Z}}{\langle e_1 * e_2, \sigma \rangle \rightarrow_{Exp} n_1 \cdot n_2}$$

$$\frac{\langle e_1, \sigma \rangle \rightarrow_{Exp} n_1 \quad \langle e_2, \sigma \rangle \rightarrow_{Exp} n_2 \quad n_i \in \mathbb{Z}, n_2 \neq 0}{\langle e_1 / e_2, \sigma \rangle \rightarrow_{Exp} n_1 \div n_2}$$

Operational Semantics: Predicates

► Expressions:

$$e ::= \dots \mid e_1 == e_2 \mid e_1 < e_2 \mid \dots \quad \langle e, \sigma \rangle \rightarrow_{Exp} b$$

► Rules:

$$\frac{\langle e_1, \sigma \rangle \rightarrow_{Exp} n_1 \quad \langle e_2, \sigma \rangle \rightarrow_{Exp} n_2 \quad n_i \in \mathbb{Z}, n_1 = n_2}{\langle e_1 == e_2, \sigma \rangle \rightarrow_{Exp} true}$$

$$\frac{\langle e_1, \sigma \rangle \rightarrow_{Exp} n_1 \quad \langle e_2, \sigma \rangle \rightarrow_{Exp} n_2 \quad n_i \in \mathbb{Z}, n_1 \neq n_2}{\langle e_1 == e_2, \sigma \rangle \rightarrow_{Exp} false}$$

$$\frac{\langle e_1, \sigma \rangle \rightarrow_{Exp} n_1 \quad \langle e_2, \sigma \rangle \rightarrow_{Exp} n_2 \quad n_i \in \mathbb{Z}, n_1 < n_2}{\langle e_1 < e_2, \sigma \rangle \rightarrow_{Exp} true}$$

$$\frac{\langle e_1, \sigma \rangle \rightarrow_{Exp} n_1 \quad \langle e_2, \sigma \rangle \rightarrow_{Exp} n_2 \quad n_i \in \mathbb{Z}, n_1 \geq n_2}{\langle e_1 < e_2, \sigma \rangle \rightarrow_{Exp} false}$$

Operational Semantics: Connectives

► Expressions:

$$e ::= \dots \mid !e \mid e_1 \ \&\& \ e_2 \mid e_1 \ || \ e_2 \quad \langle e, \sigma \rangle \rightarrow_{Exp} b$$

► Rules:

$$\frac{\langle e, \sigma \rangle \rightarrow_{Exp} true}{\langle !e, \sigma \rangle \rightarrow_{Exp} false}$$

$$\frac{\langle e, \sigma \rangle \rightarrow_{Exp} false}{\langle !e, \sigma \rangle \rightarrow_{Exp} true}$$

$$\frac{\langle e_1, \sigma \rangle \rightarrow_{Exp} false}{\langle e_1 \ \&\& \ e_2, \sigma \rangle \rightarrow_{Exp} false}$$

$$\frac{\langle e_1, \sigma \rangle \rightarrow_{Exp} true \quad \langle e_2, \sigma \rangle \rightarrow_{Exp} t}{\langle e_1 \ \&\& \ e_2, \sigma \rangle \rightarrow_{Exp} t}$$

$$\frac{\langle e_1, \sigma \rangle \rightarrow_{Exp} true}{\langle e_1 \ || \ e_2, \sigma \rangle \rightarrow_{Exp} true}$$

$$\frac{\langle e_1, \sigma \rangle \rightarrow_{Exp} false \quad \langle e_2, \sigma \rangle \rightarrow_{Exp} t}{\langle e_1 \ || \ e_2, \sigma \rangle \rightarrow_{Exp} t}$$

Questions

- ▶ Does evaluation always terminate?
- ▶ When not?
- ▶ Why not?
- ▶ Order of operands?
- ▶ Strictness?

Statements

Simple Statements

- ▶ **Core language:**
 - ▶ Assignment
 - ▶ Sequencing and empty statement — **sequences** of expressions
 - ▶ Case distinction
 - ▶ Iteration (while)
- ▶ Makes it **Turing-equivalent**
- ▶ Some languages view expressions (with side effects) as statements — and assignments as expressions

Abstract Syntax

► Statements:

$$\begin{aligned} c ::= & \mathbf{Idt} := \mathbf{Exp} \\ & | c_1; c_2 \\ & | \mathbf{nil} \\ & | \mathbf{if} (e) \mathbf{then} c_1 \mathbf{else} c_2 \\ & | \mathbf{while} (e) c \end{aligned}$$

► Operational semantics: $\langle c, \sigma \rangle \rightarrow_{Stmt} \sigma'$

Operational Semantics: Statements

► Rules:

$$\frac{\langle e, \sigma \rangle \rightarrow_{Exp} n \quad n \in \mathbb{Z}}{\langle x := e, \sigma \rangle \rightarrow_{Stmt} \sigma[x \mapsto n]} \qquad \frac{}{\langle \mathbf{nil}, \sigma \rangle \rightarrow_{Stmt} \sigma}$$
$$\frac{\langle c_1, \sigma \rangle \rightarrow_{Stmt} \sigma' \quad \langle c_2, \sigma' \rangle \rightarrow_{Stmt} \sigma''}{\langle c_1; c_2, \sigma \rangle \rightarrow_{Stmt} \sigma''}$$

► Example: $\sigma \stackrel{def}{=} \langle \rangle$

```
x  := 6;  
y  := 4 + x;
```


Operational Semantics: Statements

► Rules:

$$\frac{\langle b, \sigma \rangle \rightarrow_{Exp} true \quad \langle c_1, \sigma \rangle \rightarrow_{Stmt} \sigma'}{\langle \text{if } (b) \text{ then } c_1 \text{ else } c_2, \sigma \rangle \rightarrow_{Stmt} \sigma'}$$

$$\frac{\langle b, \sigma \rangle \rightarrow_{Exp} false \quad \langle c_2, \sigma \rangle \rightarrow_{Stmt} \sigma'}{\langle \text{if } (b) \text{ then } c_1 \text{ else } c_2, \sigma \rangle \rightarrow_{Stmt} \sigma'}$$

► Example: $\sigma \stackrel{def}{=} \langle x \mapsto 6, y \mapsto 10 \rangle$

```
if (x != 0) {  
  y := y/x;  
} else {  
  y := 0;  
}
```

Operational Semantics: Statements

► Rules:

$$\frac{\langle b, \sigma \rangle \rightarrow_{Exp} false}{\langle \mathbf{while} (b) c, \sigma \rangle \rightarrow_{Stmt} \sigma}$$
$$\frac{\langle b, \sigma \rangle \rightarrow_{Exp} true \quad \langle c, \sigma \rangle \rightarrow_{Stmt} \sigma' \quad \langle \mathbf{while} (b) c, \sigma' \rangle \rightarrow_{Stmt} \sigma''}{\langle \mathbf{while} (b) c, \sigma \rangle \rightarrow_{Stmt} \sigma''}$$

► Example: $\sigma \stackrel{def}{=} \langle x \mapsto 3 \rangle$

```
f := 1;  
while (x > 0) {  
  f := f * x;  
  x := x - 1;  
}
```

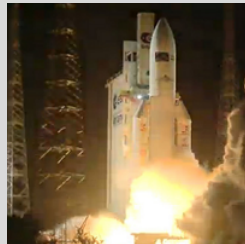
Conclusions

- ▶ **Operational semantics** describe the stepwise **evaluation** of programs by structured derivation rules.
- ▶ It gives a precise notion of **program execution** (small-step semantics), but not so much about the **meaning** of the program (big-step semantics).
- ▶ It can be used to write and in particular **verify compilers** — see next lecture.

Systems of High Safety and Security

Lecture 8 from 02.12.2025: Axiomatic Semantics: Specifying Correctness

Winter term 2025/26

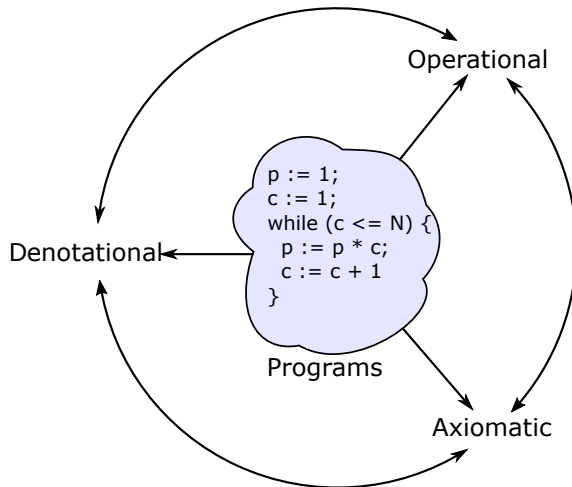


Christoph Lüth

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Three Semantics — One View



Denotational Semantics

Denotationale Semantik — Motivation

► Operationale Semantik:

Eine Menge von Regeln, die einen Zustand und ein Programm in einen neuen Zustand überführen:

$$\langle c, \sigma \rangle \rightarrow_{Stmt} \sigma'$$

► Denotationale Semantik:

Eine Menge von Regeln, die ein Programm in eine **partielle Funktion** von Zustand nach Zustand überführen

Denotat

$$\llbracket c \rrbracket_c : \Sigma \rightarrow \Sigma$$

Denotationale Semantik — Kompositionalität

- ▶ Semantik von zusammengesetzten Ausdrücken durch Kombination der Semantiken der Teilausdrücke
 - ▶ Bsp: Semantik einer Sequenz von Anweisungen durch Verknüpfung der Semantik der einzelnen Anweisungen
- ▶ Operationale Semantik ist **nicht** kompositional:

```
x= 3;  
y= x+ 7; // (*)  
z= x+ y;
```

- ▶ Semantik von Zeile (*) ergibt sich aus der Ableitung davor
- ▶ Kann nicht unabhängig abgeleitet werden

- ▶ Denotationale Semantik ist kompositional.
 - ▶ Wesentlicher Baustein: **partielle Funktionen**

Partielle Funktionen und ihre Graphen

- ▶ Der **Graph** einer partiellen Funktion $f : X \rightharpoonup Y$ ist eine Relation

$$\text{grph}(f) \subseteq X \times Y \stackrel{\text{def}}{=} \{(x, f(x)) \mid x \in \text{dom}(f)\}$$

- ▶ Wir können eine partielle Funktion durch ihren Graph definieren:

Definition (Partielle Funktion)

Eine **partielle Funktion** $f : X \rightharpoonup Y$ ist eine Relation $f \subseteq X \times Y$ so dass wenn $(x, y_1) \in f$ und $(x, y_2) \in f$ dann $y_1 = y_2$ (**Rechtseindeutigkeit**)

- ▶ Wir benutzen beide Notationen, aber für die denotationale Semantik die Graph-Notation.
- ▶ **Systemzustände** sind partielle Abbildungen $\Sigma \stackrel{\text{def}}{=} \mathbf{Loc} \rightharpoonup \mathbb{Z}$ (\longrightarrow letzte VL)

Denotierende Funktionen (Denotate)

- ▶ Arithmetische Ausdrücke: $a \in \mathbf{Exp}$ denotieren eine partielle Funktion $\Sigma \rightarrow \mathbb{Z}$
- ▶ Boolsche Ausdrücke: $b \in \mathbf{Exp}$ denotieren eine partielle Funktion $\Sigma \rightarrow \mathbb{B}$
- ▶ Anweisungen: $c \in \mathbf{Stmt}$ denotieren eine partielle Funktion $\Sigma \rightarrow \Sigma$

Denotat von arithmetischen Ausdrücken

$$\llbracket a \rrbracket_{\mathcal{A}} : \mathbf{Exp} \rightarrow (\Sigma \rightarrow \mathbb{Z})$$

$$\llbracket n \rrbracket_{\mathcal{A}} = \{(\sigma, \llbracket n \rrbracket) \mid \sigma \in \Sigma\}$$

$$\llbracket x \rrbracket_{\mathcal{A}} = \{(\sigma, \sigma(x)) \mid \sigma \in \Sigma, x \in \text{dom}(\sigma)\}$$

$$\llbracket a_0 + a_1 \rrbracket_{\mathcal{A}} = \{(\sigma, n_0 + n_1) \mid (\sigma, n_0) \in \llbracket a_0 \rrbracket_{\mathcal{A}} \wedge (\sigma, n_1) \in \llbracket a_1 \rrbracket_{\mathcal{A}}\}$$

$$\llbracket a_0 - a_1 \rrbracket_{\mathcal{A}} = \{(\sigma, n_0 - n_1) \mid (\sigma, n_0) \in \llbracket a_0 \rrbracket_{\mathcal{A}} \wedge (\sigma, n_1) \in \llbracket a_1 \rrbracket_{\mathcal{A}}\}$$

$$\llbracket a_0 * a_1 \rrbracket_{\mathcal{A}} = \{(\sigma, n_0 * n_1) \mid (\sigma, n_0) \in \llbracket a_0 \rrbracket_{\mathcal{A}} \wedge (\sigma, n_1) \in \llbracket a_1 \rrbracket_{\mathcal{A}}\}$$

$$\llbracket a_0 / a_1 \rrbracket_{\mathcal{A}} = \{(\sigma, n_0 \div n_1) \mid (\sigma, n_0) \in \llbracket a_0 \rrbracket_{\mathcal{A}} \wedge (\sigma, n_1) \in \llbracket a_1 \rrbracket_{\mathcal{A}} \wedge n_1 \neq 0\}$$

Denotat von Booleschen Ausdrücken: Relationen

$$\llbracket a \rrbracket_{\mathcal{B}} : \mathbf{Exp} \rightarrow (\Sigma \rightarrow \mathbb{B})$$

$$\llbracket true \rrbracket_{\mathcal{B}} = \{(\sigma, true) \mid \sigma \in \Sigma\}$$

$$\llbracket false \rrbracket_{\mathcal{B}} = \{(\sigma, false) \mid \sigma \in \Sigma\}$$

$$\begin{aligned} \llbracket a_0 == a_1 \rrbracket_{\mathcal{B}} = & \{(\sigma, true) \mid \sigma \in \Sigma, (\sigma, n_0) \in \llbracket a_0 \rrbracket_{\mathcal{A}}, (\sigma, n_1) \in \llbracket a_1 \rrbracket_{\mathcal{A}}, n_0 = n_1\} \\ & \cup \{(\sigma, false) \mid \sigma \in \Sigma, (\sigma, n_0) \in \llbracket a_0 \rrbracket_{\mathcal{A}}, (\sigma, n_1) \in \llbracket a_1 \rrbracket_{\mathcal{A}}, n_0 \neq n_1\} \end{aligned}$$

$$\begin{aligned} \llbracket a_0 < a_1 \rrbracket_{\mathcal{B}} = & \{(\sigma, true) \mid \sigma \in \Sigma, (\sigma, n_0) \in \llbracket a_0 \rrbracket_{\mathcal{A}}, (\sigma, n_1) \in \llbracket a_1 \rrbracket_{\mathcal{A}}, n_0 < n_1\} \\ & \cup \{(\sigma, false) \mid \sigma \in \Sigma, (\sigma, n_0) \in \llbracket a_0 \rrbracket_{\mathcal{A}}, (\sigma, n_1) \in \llbracket a_1 \rrbracket_{\mathcal{A}}, n_0 \geq n_1\} \end{aligned}$$

Denotat von Booleschen Ausdrücken: Konnektive

$$\llbracket a \rrbracket_{\mathcal{B}} : \mathbf{Exp} \rightarrow (\Sigma \rightarrow \mathbb{B})$$

$$\begin{aligned} \llbracket !b \rrbracket_{\mathcal{B}} &= \{(\sigma, true) \mid \sigma \in \Sigma, (\sigma, false) \in \llbracket b \rrbracket_{\mathcal{B}}\} \\ &\quad \cup \{(\sigma, false) \mid \sigma \in \Sigma, (\sigma, true) \in \llbracket b \rrbracket_{\mathcal{B}}\} \end{aligned}$$

$$\begin{aligned} \llbracket b_1 \ \&\& \ b_2 \rrbracket_{\mathcal{B}} &= \{(\sigma, false) \mid \sigma \in \Sigma, (\sigma, false) \in \llbracket b_1 \rrbracket_{\mathcal{B}}\} \\ &\quad \cup \{(\sigma, t_2) \mid \sigma \in \Sigma, (\sigma, true) \in \llbracket b_1 \rrbracket_{\mathcal{B}}, (\sigma, t_2) \in \llbracket b_2 \rrbracket_{\mathcal{B}}\} \end{aligned}$$

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Kompositionalität und Striktheit

Lemma (Partielle Funktion)

- i $\llbracket - \rrbracket_{\mathcal{A}}$ ist rechtseindeutig und damit eine **partielle Funktion**.
- ii $\llbracket - \rrbracket_{\mathcal{B}}$ ist rechtseindeutig und damit eine **partielle Funktion**.

- ▶ Beweis durch **strukturelle Induktion** über e .
- ▶ Ist $\llbracket - \rrbracket_{\mathcal{A}}$ strikt?

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- ▶ Sei $\llbracket b_1 \rrbracket_{\mathcal{B}}(\sigma) = false$, dann $\llbracket b_1 \ \&\& \ b_2 \rrbracket_{\mathcal{B}}(\sigma) = \llbracket b_1 \rrbracket_{\mathcal{B}}(\sigma) = false$

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- ▶ Deshalb **nicht** $\llbracket b_1 \ \&\& \ b_2 \rrbracket_{\mathcal{B}}(\sigma) = \llbracket b_1 \rrbracket_{\mathcal{B}}(\sigma) \wedge \llbracket b_2 \rrbracket_{\mathcal{B}}(\sigma)$
- ▶ Logische Operatoren müssen links nicht-strikt sein.

Denotat von Stmt

$$\llbracket \cdot \rrbracket_{\mathcal{C}} : \mathbf{Stmt} \rightarrow (\Sigma \rightarrow \Sigma)$$

$$\llbracket x = a \rrbracket_{\mathcal{C}} = \{(\sigma, \sigma[x \mapsto n]) \mid \sigma \in \Sigma \wedge (\sigma, n) \in \llbracket a \rrbracket_{\mathcal{A}}\}$$

$$\llbracket c_1; c_2 \rrbracket_{\mathcal{C}} = \llbracket c_1 \rrbracket_{\mathcal{C}} \circ \llbracket c_2 \rrbracket_{\mathcal{C}} \quad \text{Komposition von Relationen}$$

$$\llbracket \mathbf{nil} \rrbracket_{\mathcal{C}} = \mathbf{Id}_{\Sigma} \quad \mathbf{Id} := \{(\sigma, \sigma) \mid \sigma \in \Sigma\}$$

$$\begin{aligned} \llbracket \mathbf{if} (b) \mathbf{ then } c_0 \mathbf{ else } c_1 \rrbracket_{\mathcal{C}} = & \{(\sigma, \sigma') \mid (\sigma, \mathit{true}) \in \llbracket b \rrbracket_{\mathcal{B}} \wedge (\sigma, \sigma') \in \llbracket c_0 \rrbracket_{\mathcal{C}}\} \\ & \cup \{(\sigma, \sigma') \mid (\sigma, \mathit{false}) \in \llbracket b \rrbracket_{\mathcal{B}} \wedge (\sigma, \sigma') \in \llbracket c_1 \rrbracket_{\mathcal{C}}\} \end{aligned}$$

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$$\llbracket \mathbf{while} (b) c \rrbracket_c =$$

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Problem: rekursive Definition, Konstruktion über **Fixpunkt**.

Equivalence of Semantics

- Für alle $c \in \mathbf{Stmt}$, für alle Zustände σ, σ' :

$$\langle c, \sigma \rangle \rightarrow_{\mathbf{Stmt}} \sigma' \iff (\sigma, \sigma') \in \llbracket c \rrbracket_c$$

- Für alle $e \in \mathbf{Exp}$, für alle Zustände σ :

$$\langle e, \sigma \rangle \rightarrow_{\mathbf{Exp}} v \iff (\sigma, v) \in \llbracket e \rrbracket_{\mathcal{A}} (v \in \mathbb{Z})$$

$$\langle e, \sigma \rangle \rightarrow_{\mathbf{Exp}} v \iff (\sigma, v) \in \llbracket e \rrbracket_{\mathcal{B}} (v \in \mathbb{B})$$

- Beweis durch Induktion über Struktur von e, c und Ableitung von $\langle c, \sigma \rangle \rightarrow_{\mathbf{Stmt}} \sigma'$

Axiomatic Semantics

Axiomatic Semantics: Idea

- What is calculated?

```
p = 1;  
c = 1;  
while (c <= n) {  
    p = p * c;  
    c = c + 1;  
}
```

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- ▶ What is calculated? $p = n!$
- ▶ Why? How can we **prove** it?

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- ▶ Operational/denotational semantics not suitable for **correctness proofs**.
- ▶ Basic principle:
 - 1 Abstraction
 - 2 State-dependent **assertions**
 - 3 Calculating validity of assertions by **rules**.

Foundations of Axiomatic Semantics

```
// (A)
p = 1;
c = 1;
// (B)
while (c <= n) {
    // (C)
    p = p * c;
    c = c + 1;
    // (D)
}
// (E)
```

- ▶ **Zusicherungen** über den Zustand
- ▶ Beispiele:
 - ▶ (B): Hier gilt $p = c = 1$
 - ▶ (D): Hier ist c um eines größer als der Wert von c an Punkt (C)
- ▶ Gesamtaussage: Wenn bei (A) der Wert von $n \geq 0$ ist, dann ist bei (E) $p = n!$

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- ▶ Beobachtung:
 - ▶ n ist eine "Eingabevariable", der Wert am Anfang des Programmes (A) ist relevant;

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- ▶ Beobachtung:
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- ▶ Gesamtaussage: Wenn bei (A) der Wert von $n \geq 0$ ist, dann ist bei (E) $p = n!$
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 - ▶ n ist eine "Eingabevariable", der Wert am Anfang des Programmes (A) ist relevant;
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 - ▶ c ist eine "Arbeitsvariable", der Wert am Anfang und Ende ist irrelevant

Was berechnet dieses Programm?

```
// (A)
x= 1;
c= 1;
// (B)
while (c <= y) {
    // (C)
    x= 2*x;
    c= c+1;
    // (D)
}
// (E)
```

Betrachtet nebenstehendes Programm.

Analog zu dem Beispiel auf der vorherigen Folie:

- 1 Was berechnet das Programm?
- 2 Welches sind "Eingabevariablen", welches "Ausgabevariablen", welches sind "Arbeitsvariablen"?
- 3 Welche Zusicherungen und Zusammenhänge gelten zwischen den Variablen an den Punkten (A) bis (E)?

Towards Axiomatic Semantics

- ▶ Kern der Floyd-Hoare-Logik sind **zustandsabhängige Aussagen**
- ▶ Aber: wie können wir Aussagen **jenseits** des Zustandes treffen?
- ▶ Einfaches Beispiel:

```
x = x + 1;
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- ▶ Der Wert von x wird um 1 erhöht
- ▶ Der Wert von x ist hinterher größer als vorher

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- ▶ Der Wert von x wird um 1 erhöht
- ▶ Der Wert von x ist hinterher größer als vorher
- ▶ Wir benötigen **zustandsfreie** Aussagen, um von Zuständen unabhängig **vergleichen** zu können.
- ▶ Die Logik **abstrahiert** den Effekt von Programmen.

Basic Building Blocks

- ▶ **Logische Variablen** (zustandsfrei) und **Programmvariablen** (zustandsabhängig)
- ▶ **Zusicherungen** mit logischen und Programmvariablen
- ▶ **Floyd-Hoare-Tripel** $\{P\} c \{Q\}$
 - ▶ Vorbedingung P (Zusicherung)
 - ▶ Programm c
 - ▶ Nachbedingung Q (Zusicherung)
- ▶ Floyd-Hoare-Logik abstrahiert von Programmen zu logischen Formeln.

Assertions

- Erweiterung von **Exp** durch

- **Logische** Variablen **Var**

- Definierte Funktionen und Prädikate

- Implikation und Quantoren

$v := N, M, L, U, V, X, Y, Z$

$n!, x^y, \dots$

$b_1 \longrightarrow b_2, \forall v. b, \exists v. b$

- Formal:

Aexpv $a ::= \mathbb{Z} \mid \mathbf{Idt} \mid \mathbf{Var} \mid a_1 + a_2 \mid a_1 - a_2 \mid a_1 \times a_2 \mid a_1 / a_2$
 $\mid f(e_1, \dots, e_n)$

Assn $b ::= \mathbf{true} \mid \mathbf{false} \mid a_1 = a_2 \mid a_1 \leq a_2$
 $\mid \neg b \mid b_1 \wedge b_2 \mid b_1 \vee b_2$
 $\mid b_1 \longrightarrow b_2 \mid p(e_1, \dots, e_n) \mid \forall v. b \mid \exists v. b$

Denotationale Semantik von Zusicherungen

- Erste Näherung: Funktion

$$\llbracket a \rrbracket_{\mathcal{A}} : \mathbf{Aexpv} \rightarrow (\Sigma \multimap \mathbb{Z})$$

$$\llbracket b \rrbracket_{\mathcal{B}} : \mathbf{Assn} \rightarrow (\Sigma \multimap \mathbb{B})$$

- **Konservative** Erweiterung von $\llbracket a \rrbracket_{\mathcal{A}} : \mathbf{Exp} \rightarrow (\Sigma \multimap \mathbb{Z})$
- Aber: was ist mit den logischen Variablen?

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- ▶ **Konservative** Erweiterung von $\llbracket a \rrbracket_{\mathcal{A}} : \mathbf{Exp} \rightarrow (\Sigma \rightarrow \mathbb{Z})$
- ▶ Aber: was ist mit den logischen Variablen?
- ▶ Zusätzlicher Parameter **Belegung** der logischen Variablen $I : \mathbf{Var} \rightarrow \mathbb{Z}$

$$\llbracket a \rrbracket_{\mathcal{A}} : \mathbf{Aexpv} \rightarrow (\mathbf{Var} \rightarrow \mathbb{Z}) \rightarrow (\Sigma \rightarrow \mathbb{Z})$$

$$\llbracket b \rrbracket_{\mathcal{B}} : \mathbf{Assn} \rightarrow (\mathbf{Var} \rightarrow \mathbb{Z}) \rightarrow (\Sigma \rightarrow \mathbb{B})$$

- ▶ Bemerkung: $I : \mathbf{Var} \rightarrow \mathbb{Z}$ ist immer eine **totale Funktion** im Gegensatz zu einem Zustand.

Denotat von Exp

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Denotat von Aexpv

$$\llbracket a \rrbracket_{\mathcal{A}} : \mathbf{Aexpv} \rightarrow (\mathbf{Var} \rightarrow \mathbb{Z}) \rightarrow \rightarrow (\Sigma \rightarrow \mathbb{Z})$$

Sei $\mathcal{I} : \mathbf{Var} \rightarrow \mathbb{Z}$ eine beliebige Belegung

$$\llbracket n \rrbracket_{\mathcal{A}}^{\mathcal{I}} = \{(\sigma, \llbracket n \rrbracket) \mid \sigma \in \Sigma\}$$

$$\llbracket x \rrbracket_{\mathcal{A}}^{\mathcal{I}} = \{(\sigma, \sigma(x)) \mid \sigma \in \Sigma, x \in \text{dom}(\sigma)\}$$

$$\llbracket a_0 + a_1 \rrbracket_{\mathcal{A}}^{\mathcal{I}} = \{(\sigma, n_0 + n_1) \mid (\sigma, n_0) \in \llbracket a_0 \rrbracket_{\mathcal{A}}^{\mathcal{I}} \wedge (\sigma, n_1) \in \llbracket a_1 \rrbracket_{\mathcal{A}}^{\mathcal{I}}\}$$

$$\llbracket a_0 - a_1 \rrbracket_{\mathcal{A}}^{\mathcal{I}} = \{(\sigma, n_0 - n_1) \mid (\sigma, n_0) \in \llbracket a_0 \rrbracket_{\mathcal{A}}^{\mathcal{I}} \wedge (\sigma, n_1) \in \llbracket a_1 \rrbracket_{\mathcal{A}}^{\mathcal{I}}\}$$

$$\llbracket a_0 * a_1 \rrbracket_{\mathcal{A}}^{\mathcal{I}} = \{(\sigma, n_0 \times n_1) \mid (\sigma, n_0) \in \llbracket a_0 \rrbracket_{\mathcal{A}}^{\mathcal{I}} \wedge (\sigma, n_1) \in \llbracket a_1 \rrbracket_{\mathcal{A}}^{\mathcal{I}}\}$$

$$\llbracket a_0 / a_1 \rrbracket_{\mathcal{A}}^{\mathcal{I}} = \{(\sigma, n_0 \div n_1) \mid (\sigma, n_0) \in \llbracket a_0 \rrbracket_{\mathcal{A}}^{\mathcal{I}} \wedge (\sigma, n_1) \in \llbracket a_1 \rrbracket_{\mathcal{A}}^{\mathcal{I}} \wedge n_1 \neq 0\}$$

$$\llbracket X \rrbracket_{\mathcal{A}}^{\mathcal{I}} = \{(\sigma, \mathcal{I}(X)) \mid \sigma \in \Sigma, X \in V\}$$

Erfüllung von Zusicherungen

- ▶ Wann gilt eine Zusicherung $b \in \mathbf{Assn}$ in einem Zustand σ ?
 - ▶ Auswertung (denotationale Semantik) ergibt *true*
 - ▶ Belegung ist zusätzlicher Parameter

Erfülltheit von Zusicherungen

$b \in \mathbf{Assn}$ ist in Zustand σ mit Belegung l erfüllt ($\sigma \models^l b$), gdw

$$\llbracket b \rrbracket_{\mathcal{B}}^l(\sigma) = \textit{true}$$

Floyd-Hoare-Tripel

Partielle Korrektheit ($\models \{P\} c \{Q\}$)

$\{P\} c \{Q\}$ ist **partiell korrekt**, wenn für all Belegungen I und alle Zustände σ , die P erfüllen, gilt: **wenn** die Ausführung von c mit σ in einem Zustand τ terminiert, **dann** erfüllt τ mit Belegung I Q .

$$\models \{P\} c \{Q\} \iff \forall I. \forall \sigma. \sigma \models^I P \wedge \exists \tau. (\sigma, \tau) \in \llbracket c \rrbracket_c \longrightarrow \tau \models^I Q$$

- Gleiche Belegung der logischen Variablen in P und Q erlaubt **Vergleich** zwischen Zuständen

Totale Korrektheit ($\models [P] c [Q]$)

$[P] c [Q]$ ist **total korrekt**, wenn für all Belegungen I und alle Zustände σ , die P erfüllen, die Ausführung von c mit σ in einem Zustand τ terminiert, und τ mit der Belegung I erfüllt Q .

$$\models [P] c [Q] \iff \forall I. \forall \sigma. \sigma \models^I P \longrightarrow \exists \tau. (\sigma, \tau) \in \llbracket c \rrbracket_c \wedge \tau \models^I Q$$

Beispiele

► Folgendes **gilt**:

$$\models \{true\} \textbf{while}(1)\{ \} \{true\}$$

Beispiele

- ▶ Folgendes **gilt**:

$$\models \{true\} \textbf{while}(1)\{ \} \{true\}$$

- ▶ Folgendes gilt **nicht**:

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Beispiele

- ▶ Folgendes **gilt**:

$$\models \{true\} \text{ while}(1)\{ \} \{true\}$$

- ▶ Folgendes gilt **nicht**:

$$\models [true] \text{ while}(1)\{ \} [true]$$

- ▶ Folgende **gelten**:

$$\models \{false\} \text{ while } (true) \text{ nil } \{true\}$$

$$\models [false] \text{ while } (true) \text{ nil } [true]$$

Wegen *ex falso quodlibet*: $false \longrightarrow \phi$

Gültigkeit und Herleitbarkeit

- ▶ **Semantische Gültigkeit:** $\models \{P\} c \{Q\}$

- ▶ Definiert durch denotationale Semantik:

$$\models \{P\} c \{Q\} \iff \forall I. \forall \sigma. \sigma \models^I P \wedge \exists \tau. (\sigma, \tau) \in \llbracket c \rrbracket_c \longrightarrow \tau \models^I Q$$

- ▶ Problem: müssten Semantik von c ausrechnen

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- Problem: müssten Semantik von c ausrechnen

► **Syntaktische Herleitbarkeit:** $\vdash \{P\} c \{Q\}$

- Durch **Regeln** definiert

- Kann **hergeleitet** werden

- Muss **korrekt** bezüglich semantischer Gültigkeit gezeigt werden

► Generelles Vorgehen in der Logik — **nächste Vorlesung**